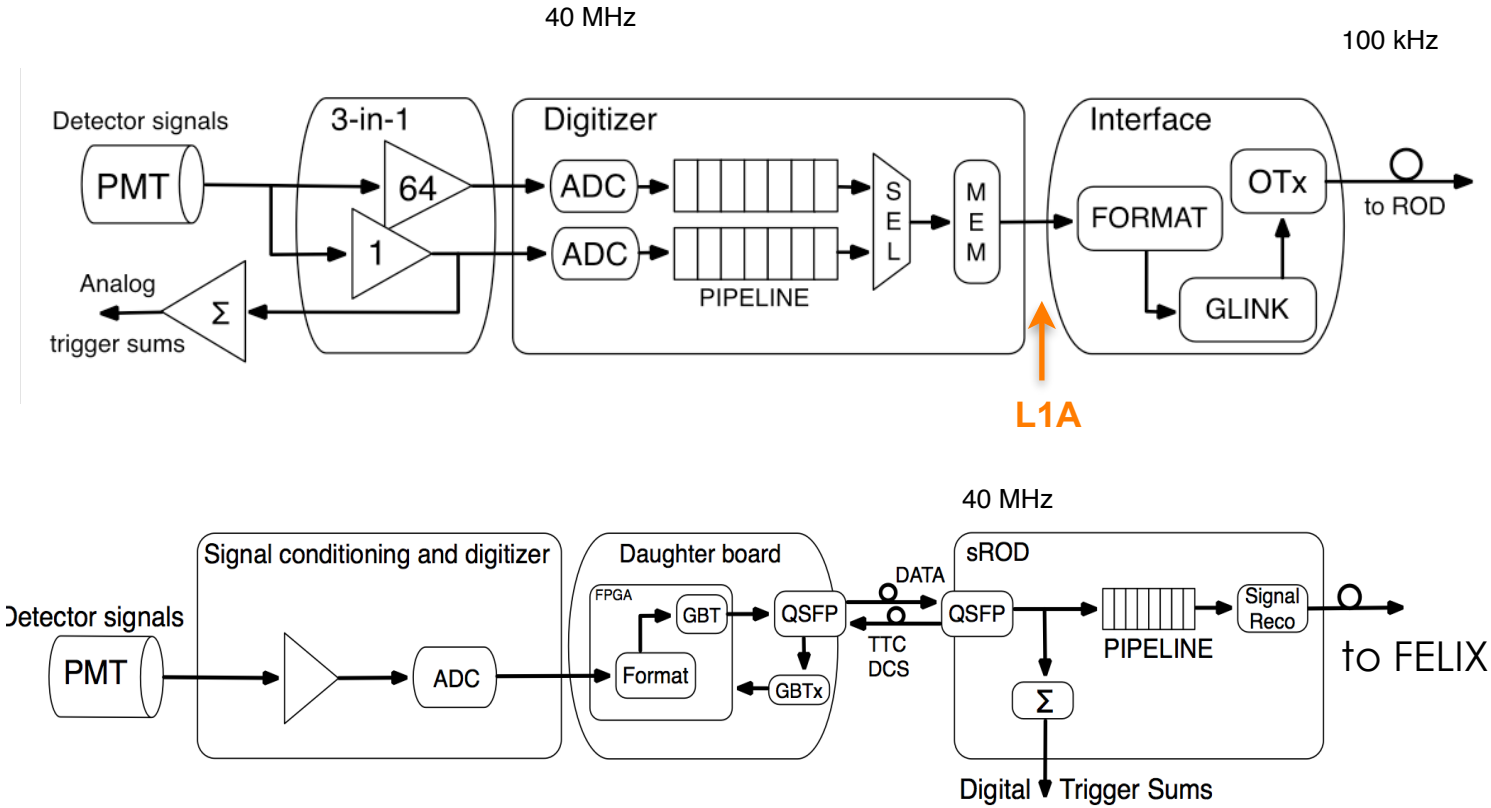
Tile Calorimeter Demonstrator project Status and Plans

Giulio Usai

U.Texas at Arlington

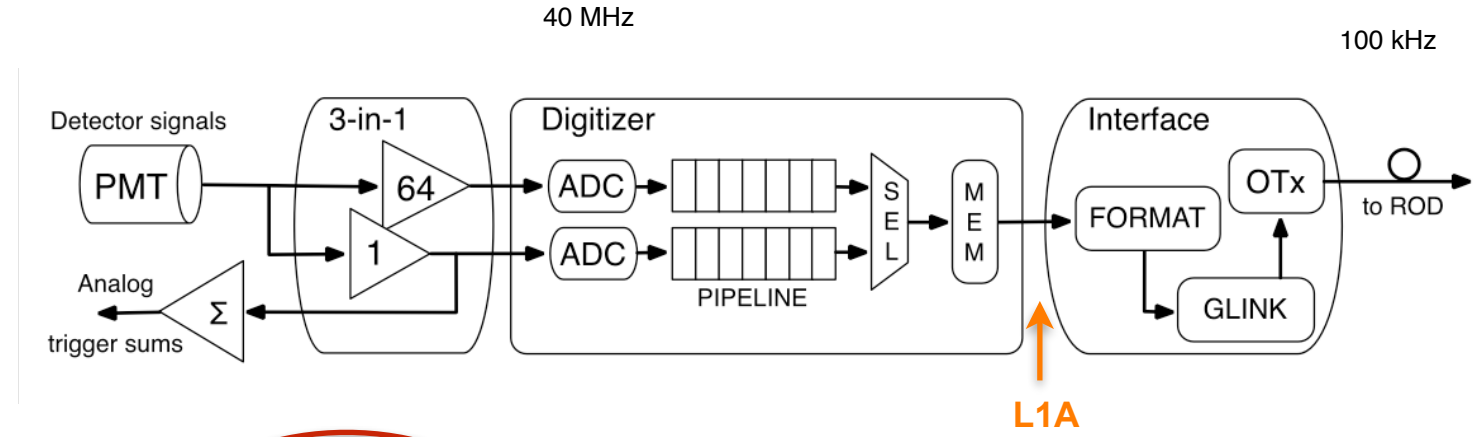
Motivations: read out architecture

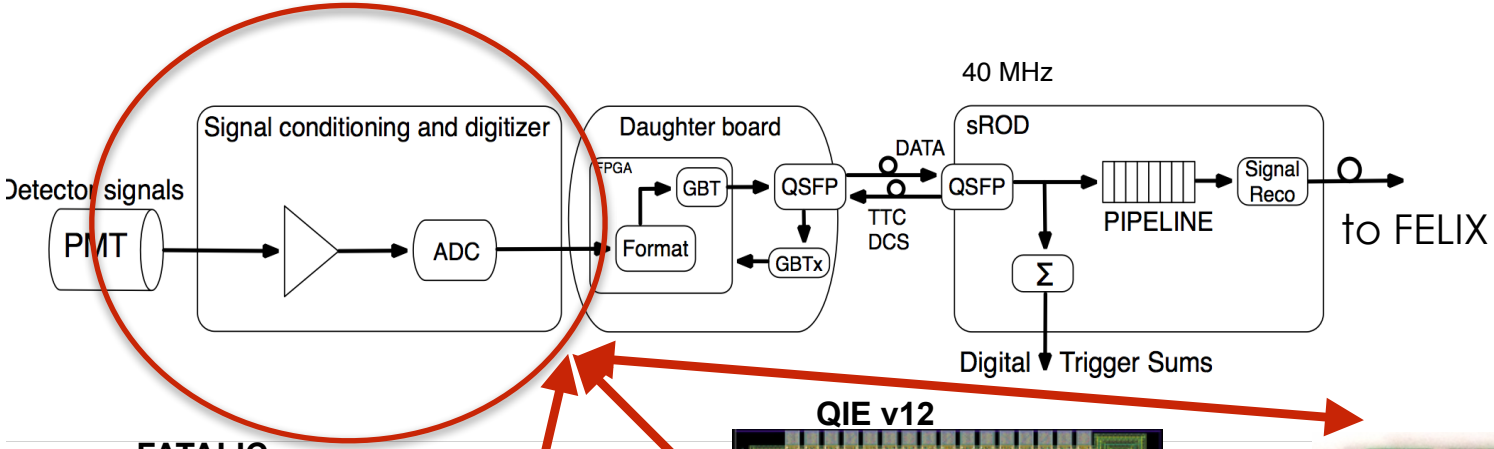


Up Link only	Present	Upgrade
Total BW	***~ 165 Gbps***	***~80 Tbps***
Nb fibers	256	8192
Fiber BW	***640 Mbps***	***10 Gbps***
Nb RODs	32	32?
ROD Crates	***4***	***4***
In BW/ROD	5 Gbps	2 Tbps
Out BW/ROD ***DAQ***	***2,56 Gbps***	***~ 20 Gbps***
Out BW/ROD $_{L1}$	Analog FE	< 80 Gbps

- Complete replacement of on-detector and off-detector electronics
- New readout strategy to provide digital trigger information at low latency for L0/L1
  - Pipelines, derandomizers, DCS&TTC interface moved off-detector

Motivations: read out architecture





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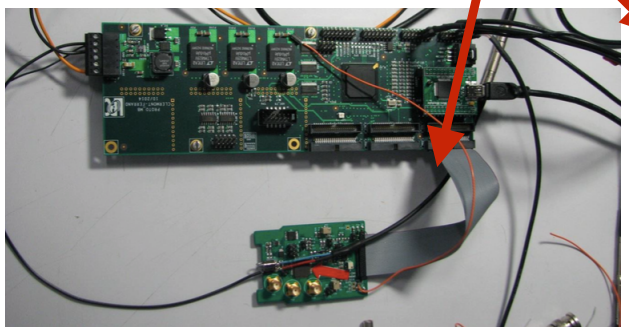
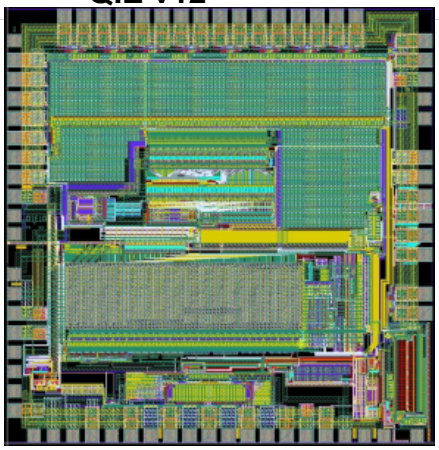
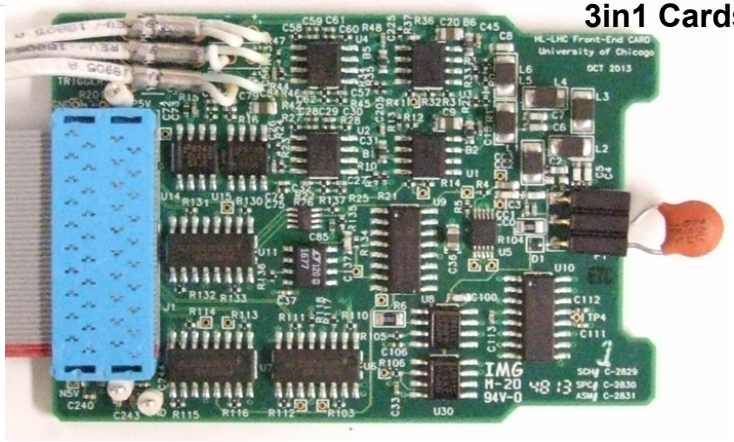
FATALIC



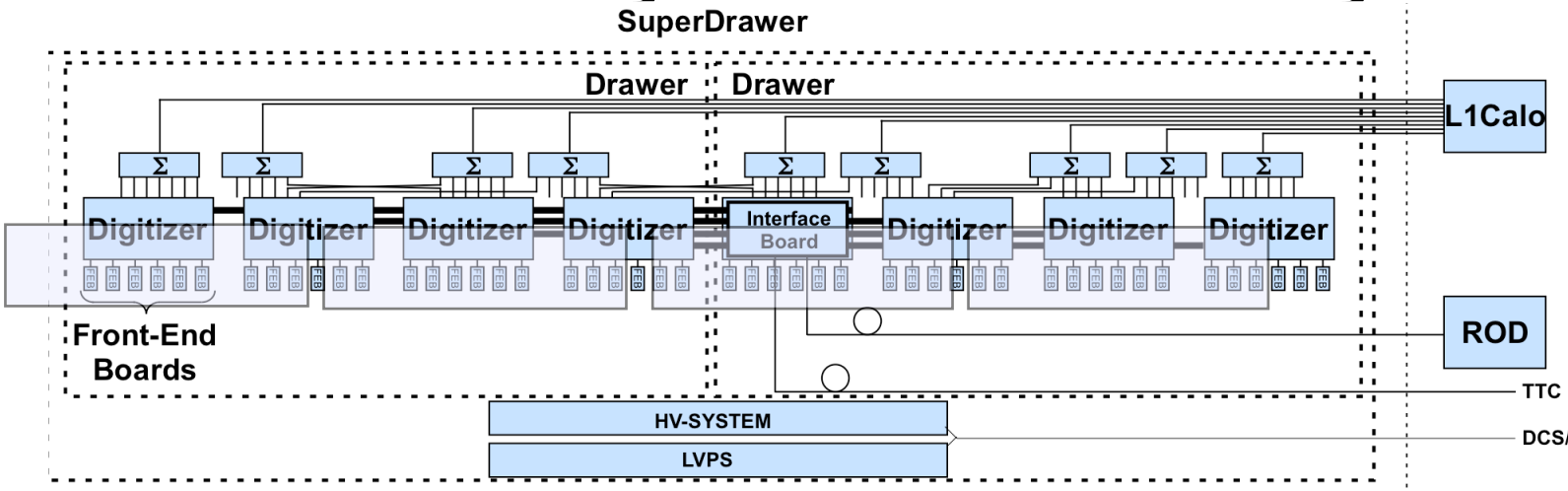
QIE v12



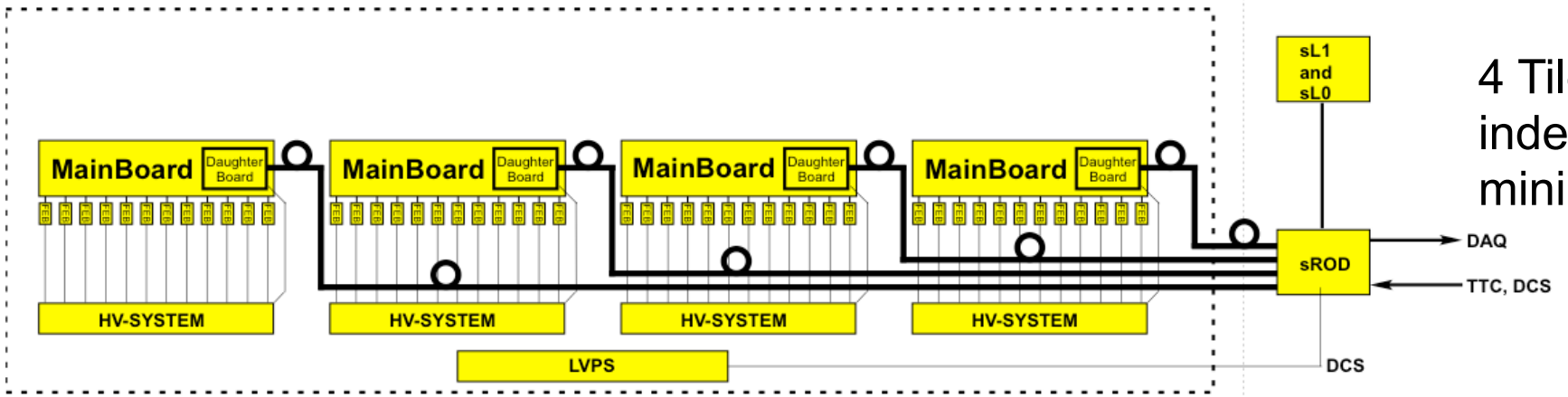
3in1 Cards



Motivations: system modularity



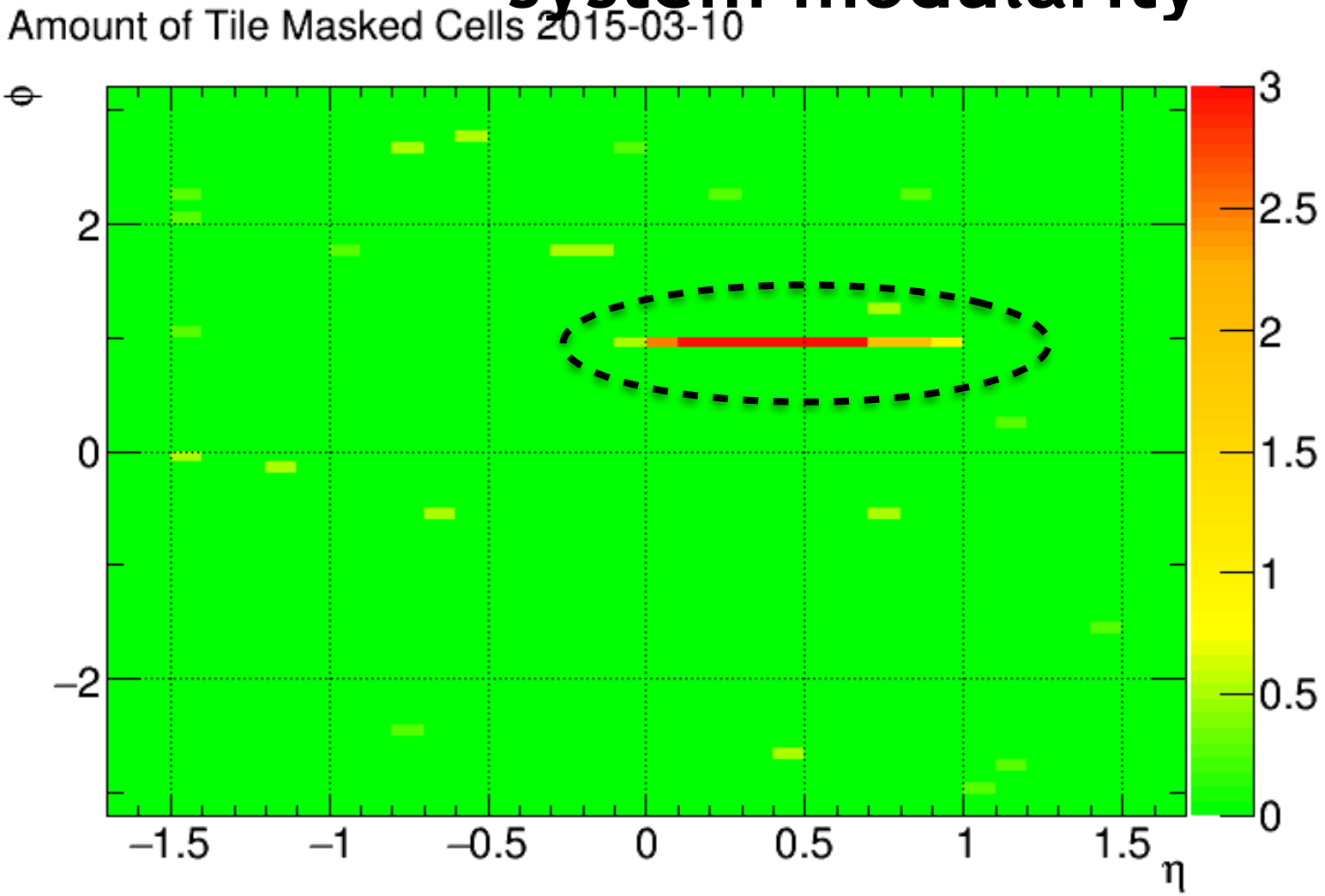
1 Tile Super Drawer



4 Tile independent mini Drawers

- improve reliability: reduce interconnections and stack of boards, implement redundancy
- minimise impact of failures with smaller DAQ elements: 1 SD is split in 4 independent mini-drawers with full redundant data path and powering

Motivations: system modularity



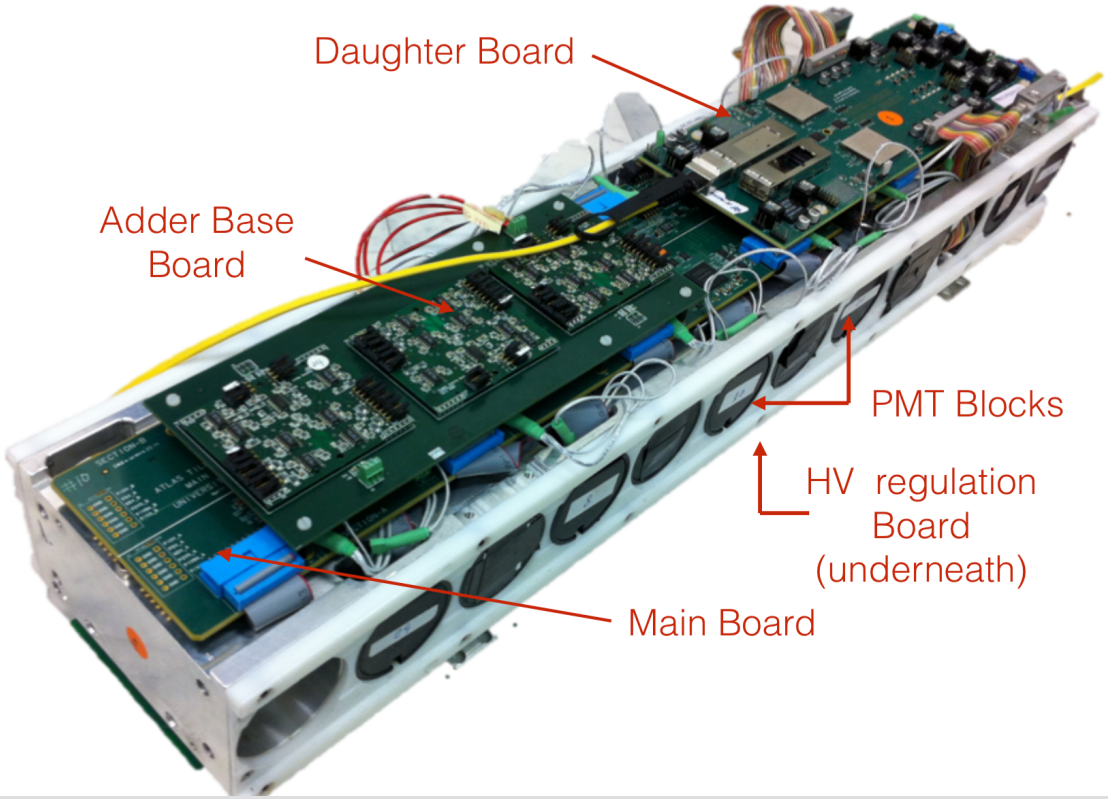
1 Super Drawer
~3 m long

4 independent mini Drawers
~75 cm each

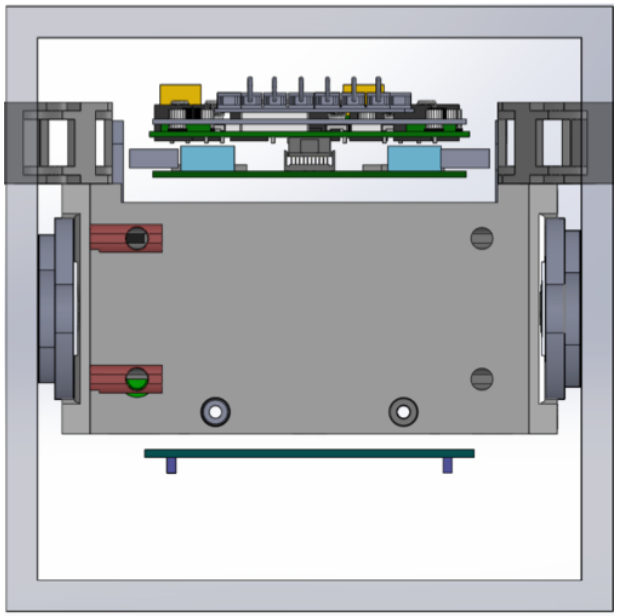
- improve reliability: reduce interconnections and stack of boards, implement redundancy
- minimise impact of failures with smaller DAQ elements: 1 SD is split in 4 independent mini-drawers with full redundant data path and powering

Better access: mini-drawers

- Smaller elements simplify the handling during maintenance and allow access in reduced detector opening (ATLAS standard opening).
- Each mini-drawer have 2 independent read-out sections:
  - 12 PMTs and 12 FE boards reading out 6 cells.
  - 1 main-board for FE boards services
  - 1 daughter-board: Optical Interface with the BE
  - 1 HV regulation board
  - 1 adder base board + 3 adder cards: trigger analog signals for hybrid demonstrator



Cross section of a mini-drawer



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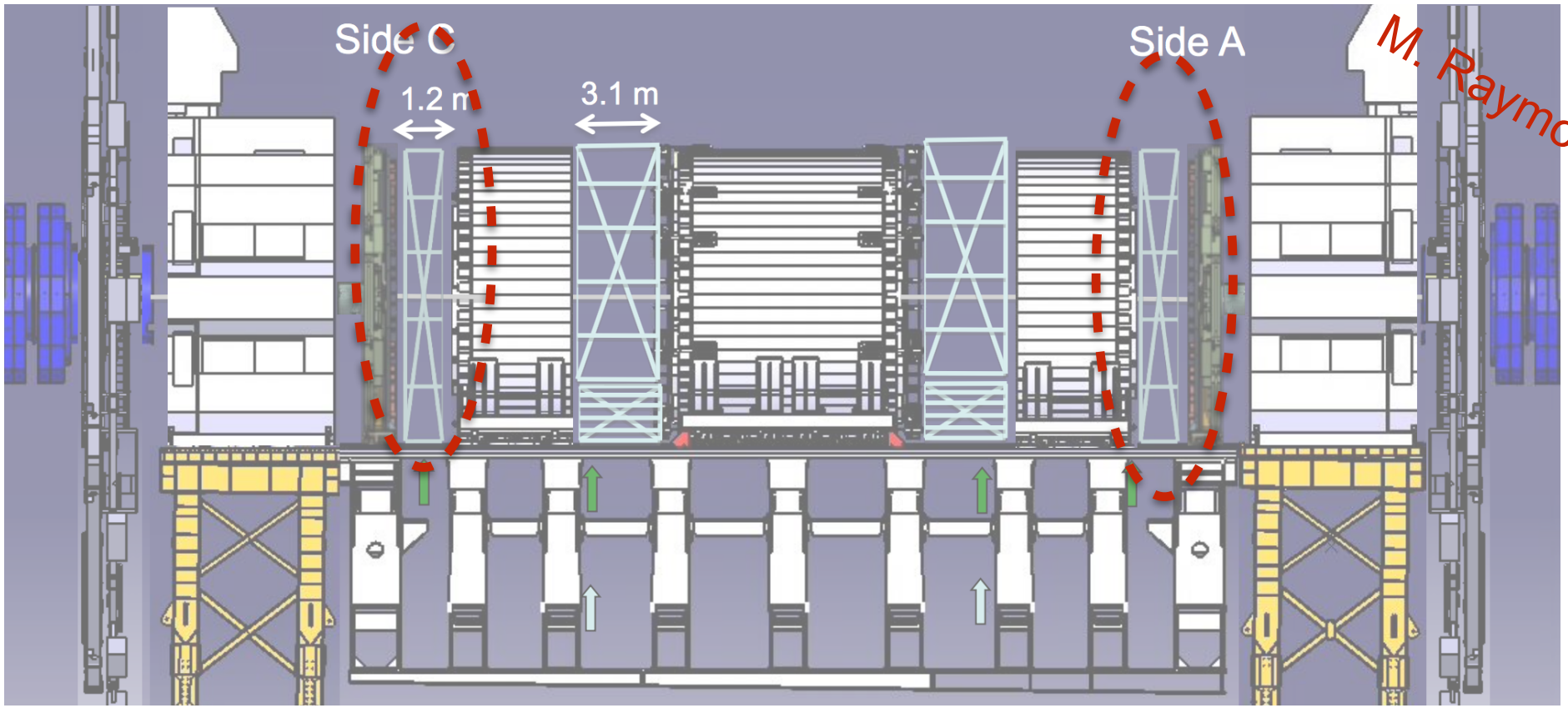

Full redundancy in the read out

- Smaller elements simplify the handling during maintenance and allow access in reduced detector opening (ATLAS standard opening).
- Each mini-drawer have 2 independent read-out sections: fully redundant cell read-out
  - 12 PMTs and 12 FE boards reading out 6 cells.
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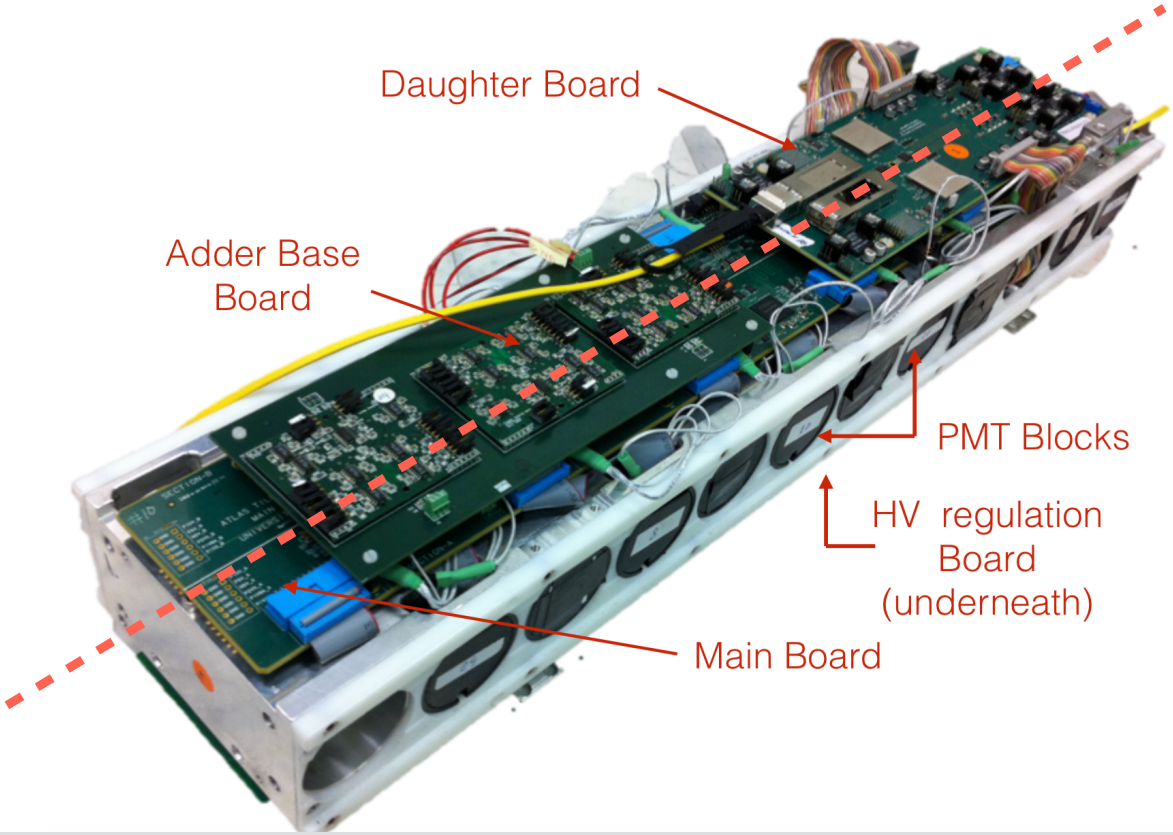
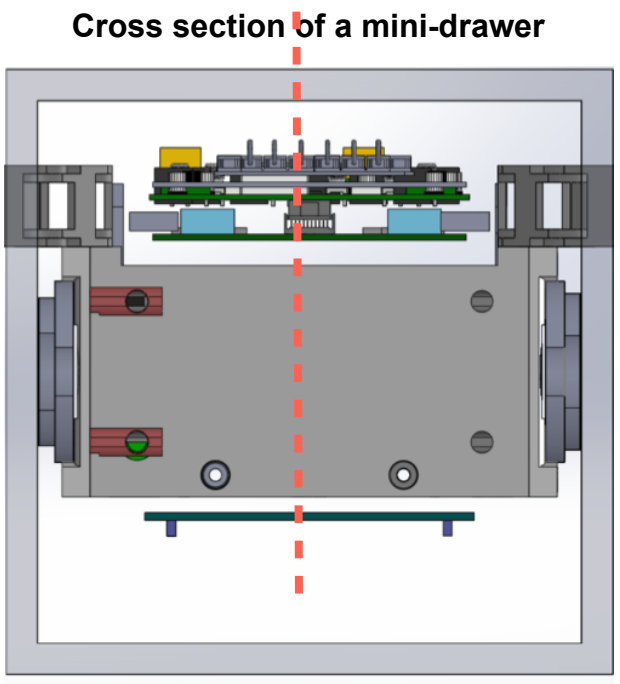
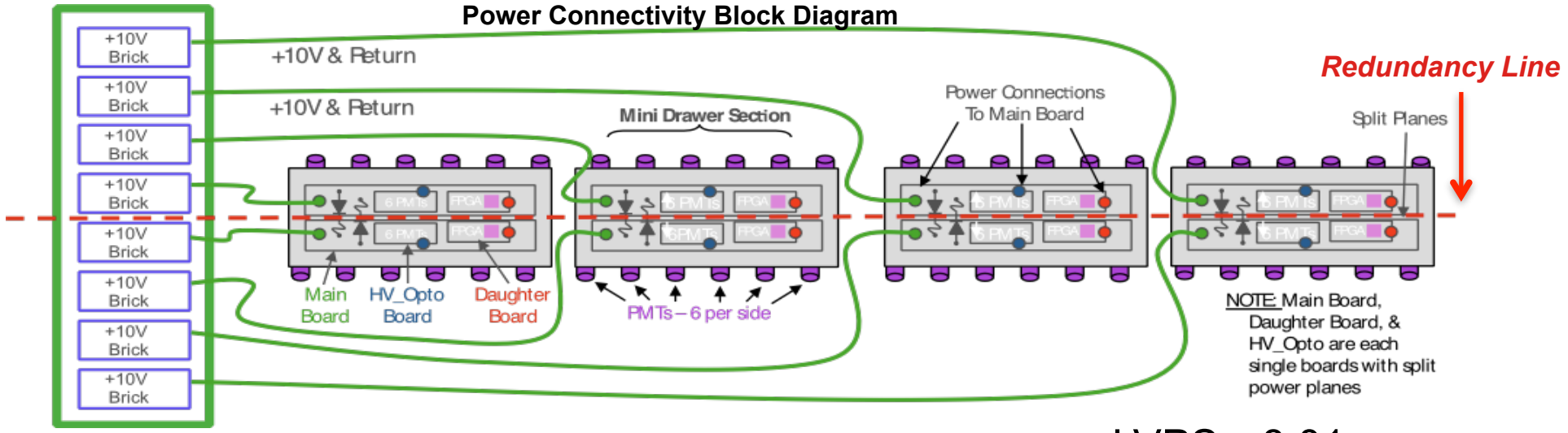


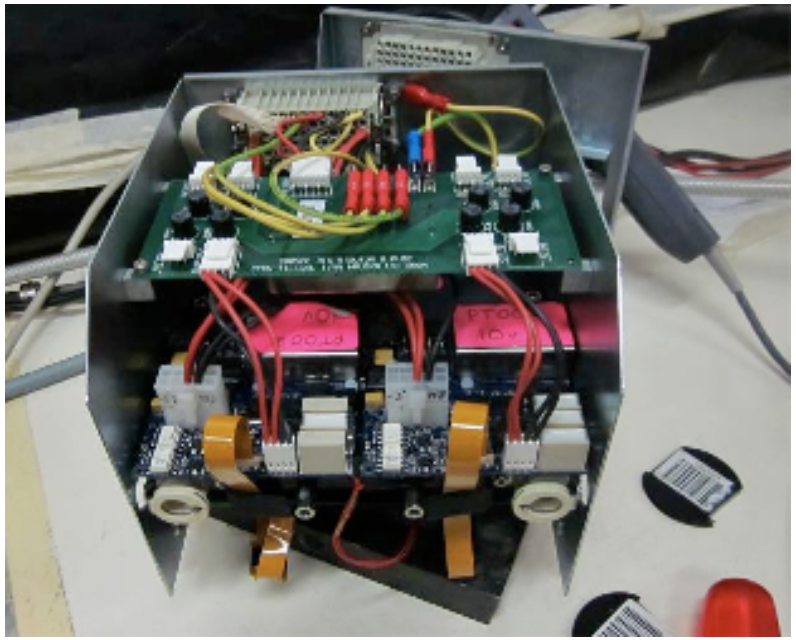


Full redundancy in power distr.



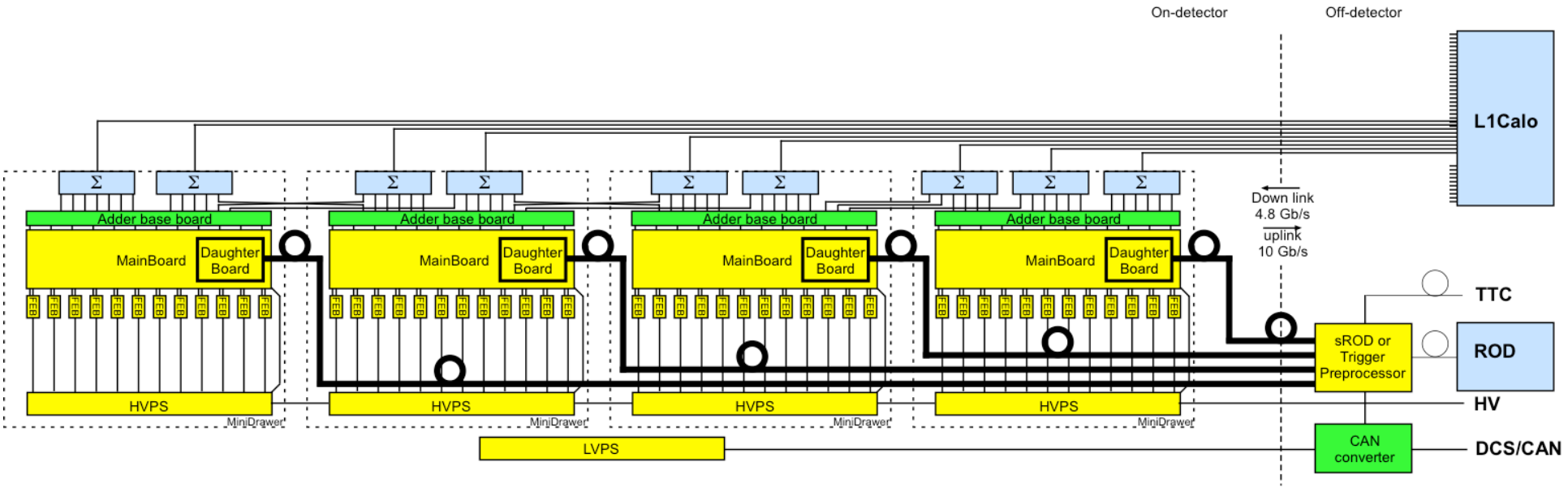
- three stage power distribution system
- bulk 200VDC PS in USA15
- "finger LVPS": based on the used DC/DC converter
  - 8 separate units providing only +10V
  - Each unit power half a mini-drawer but can power both for redundancy (diode OR)
- Point-of-Load regulators
  - mounted on Main Board, Daughter Board and HV Opto
  - Completed TID tests on 5 COTS regulators, marginal results for -5V regulator
  - NIEL and SEU tested

LVPS v.8.01



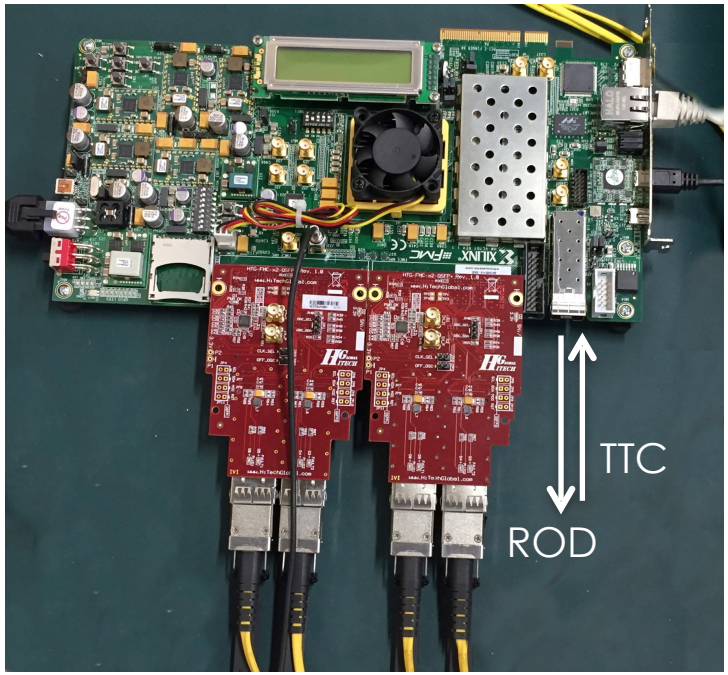
Tile FE module demonstrator

- Hybrid prototype we plan integrate into ATLAS to evaluate the new architecture.
  - similar to the phase-II system but fully compatibility with the current system (use the 3in1 FE option).
    - receive TTC/CANbus commands from sROD
    - send data to the ROD trough the sROD
    - provide both analog/digital trigger output



Back end electronics:sROD demonstrator

Super-ROD prototype

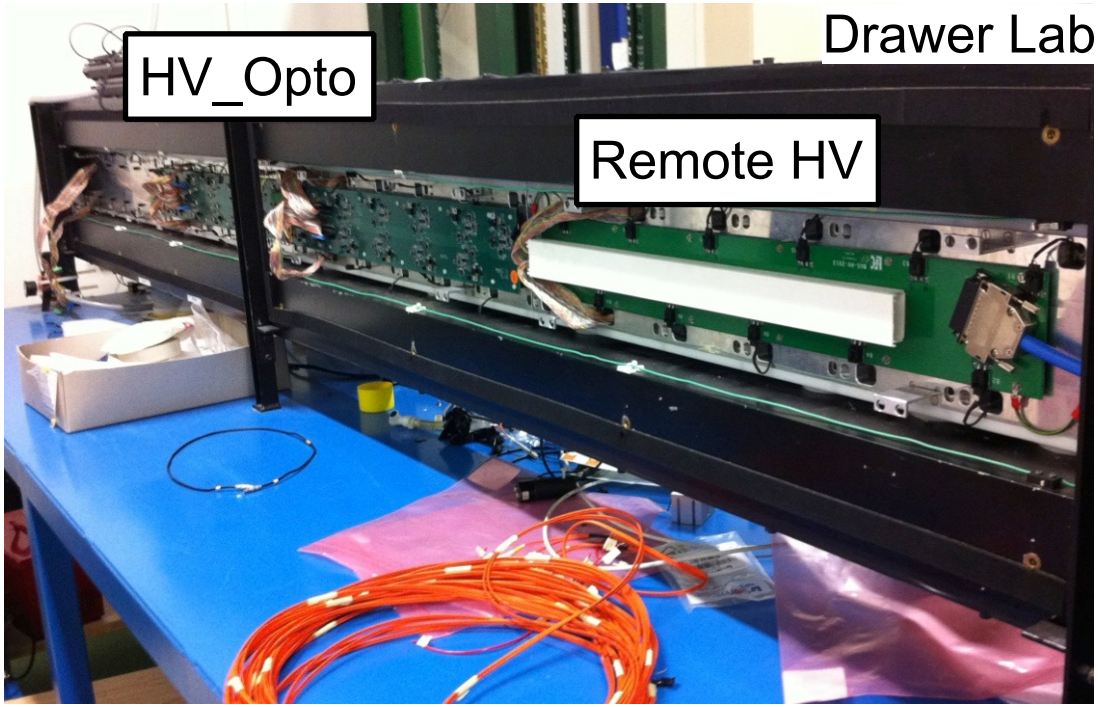


commercial emulator vc707+QSFP-FMC

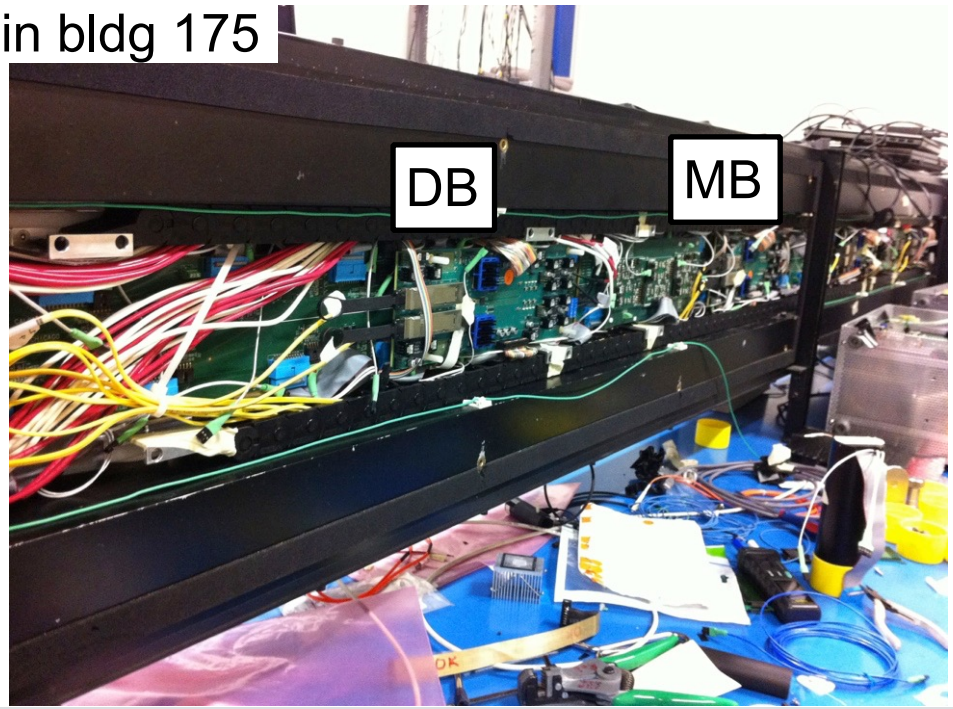
- first prototype designed and constructed (mid size AMC:180.6 mm x 148.5 mm)
- now fully functional
- development of firmware is well advanced using the VC707 emulator.
- now firmware migration and integration in the ATCA for the TB in October

Tile demonstrator setup @ CERN

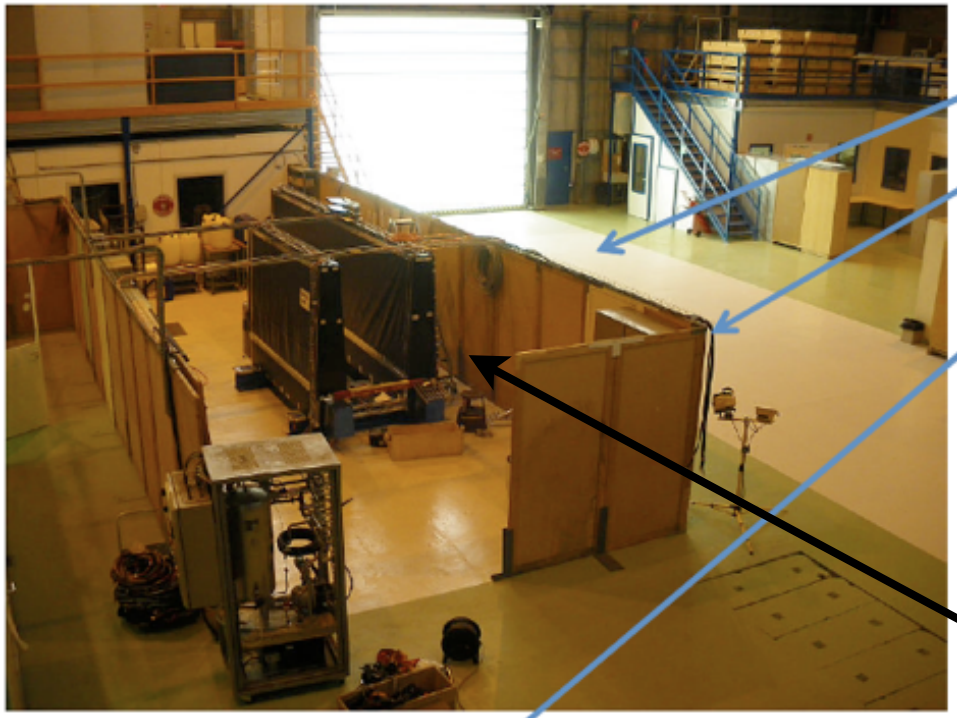
- full system with 4 mini-drawers and DAQ using a VC707.
  - Calibration data acquired routinely: CIS, LED pulses, pedestal runs.
- data storage in eos and automatic reconstruction and plotting
- powered with LVPS v.8.01 and the two HV regulation options being evaluated.
- DCS communication via sROD interface being implemented

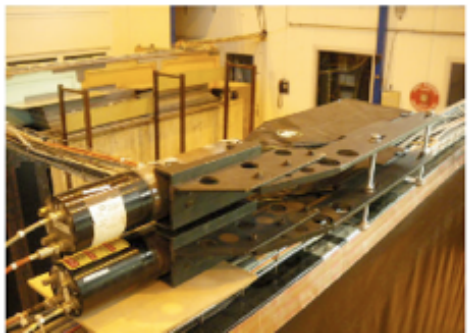


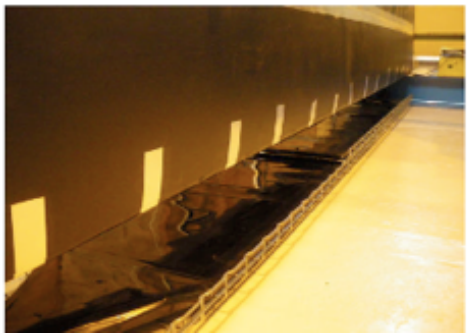
Drawer Lab in bldg 175

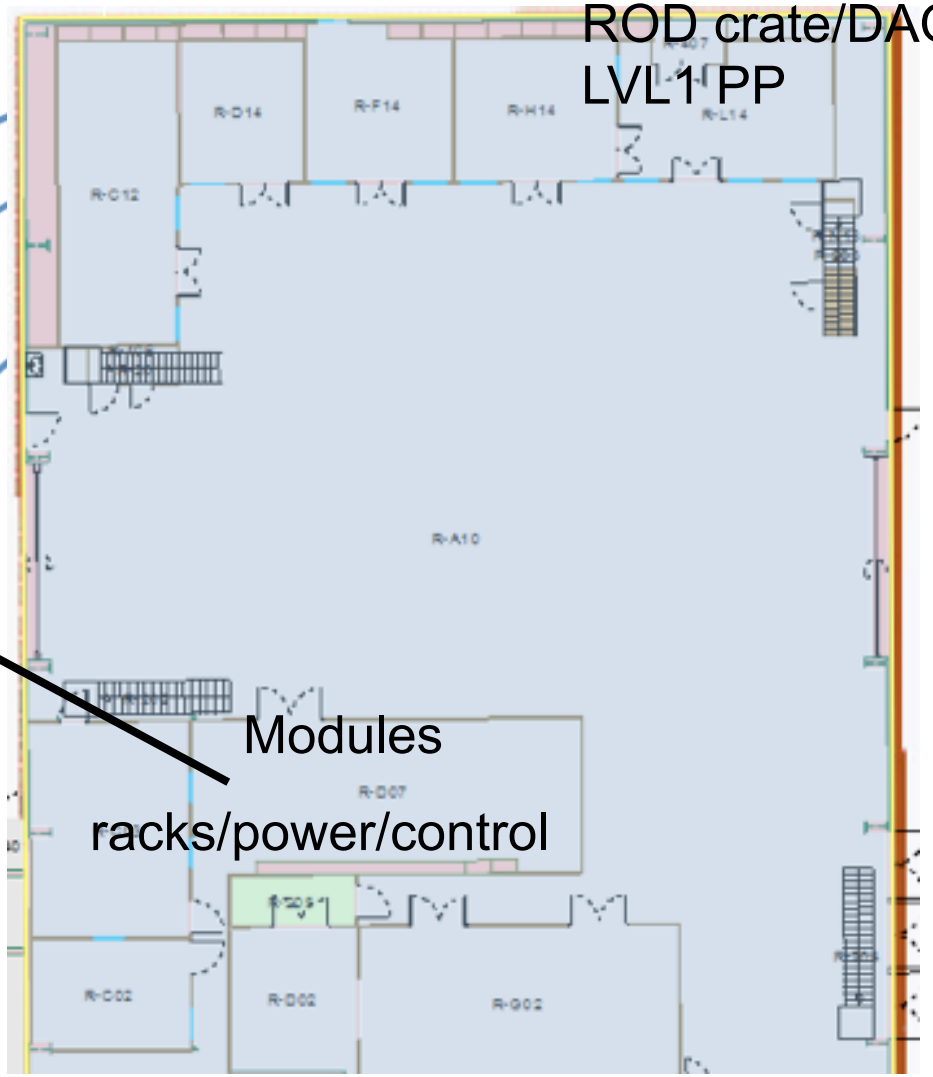


Tile slice in bldg. 175@CERN



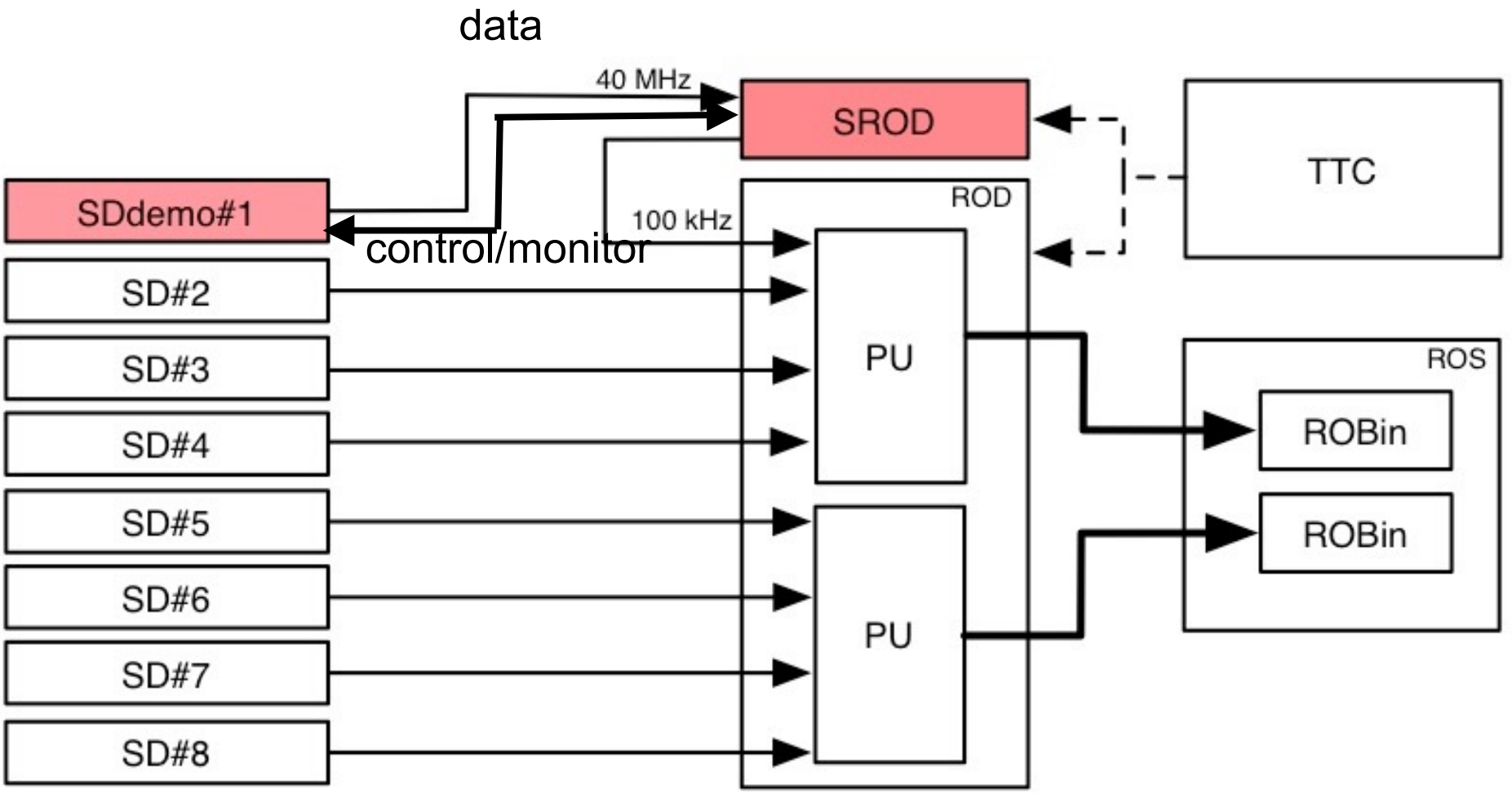






integration with ATLAS DAQ

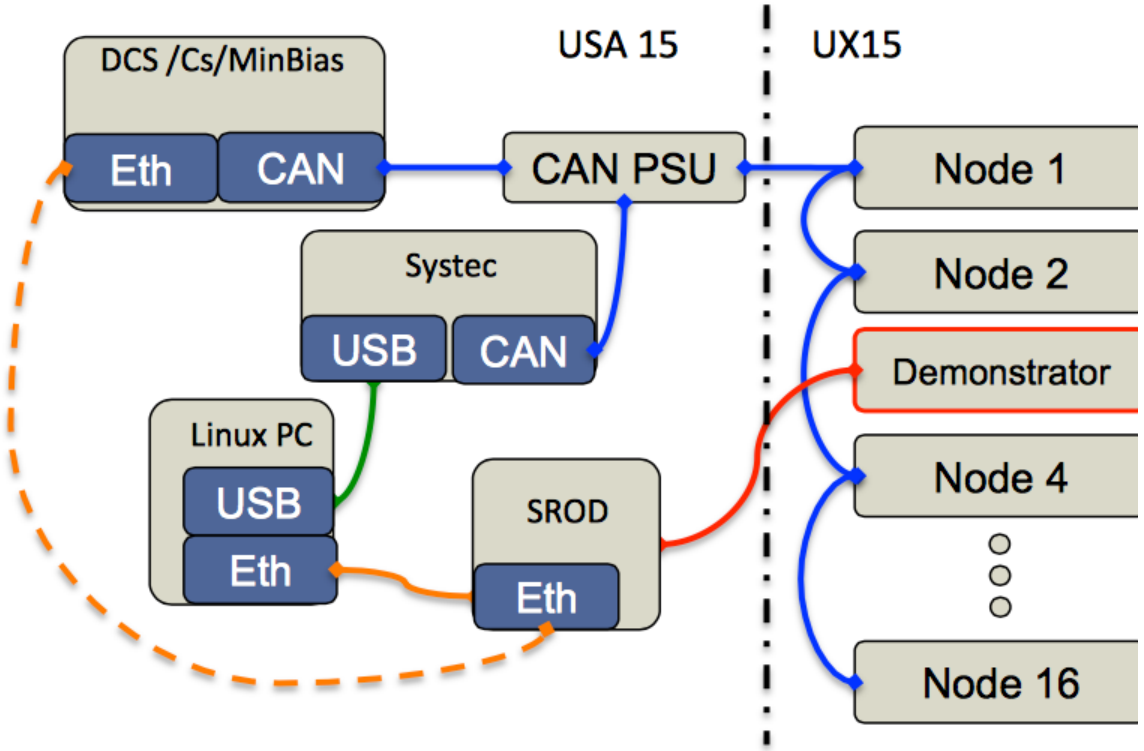
TTC/DataFlow

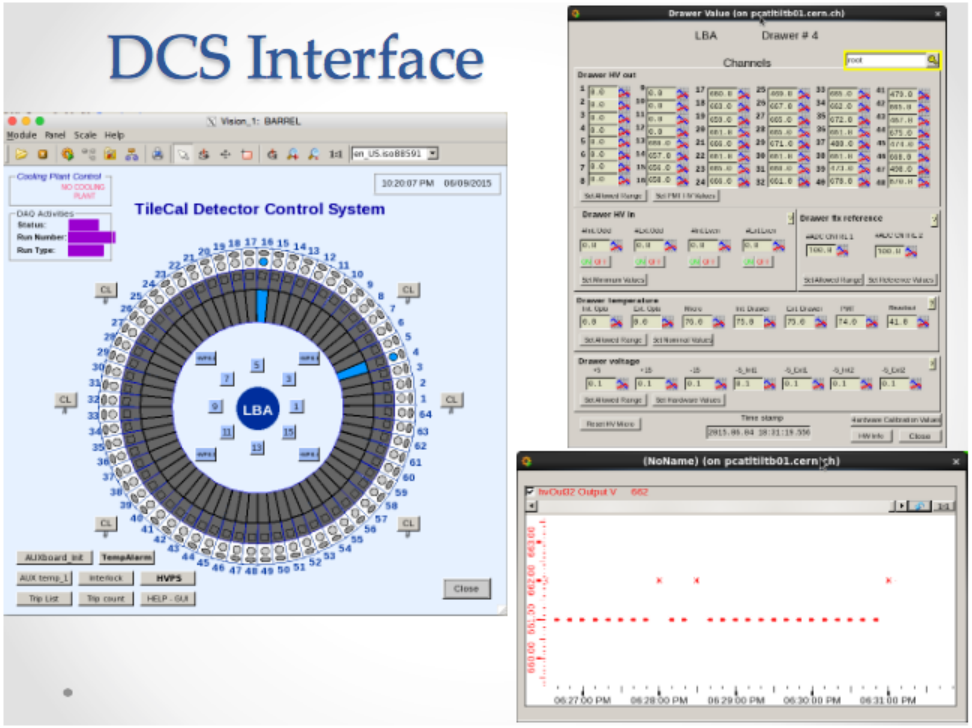


Integration with DCS

- DCS for demonstrator working
- GUI updates being discussed
- Installation on ATCA CPU ongoing
- Usage of IP bus hub foreseen

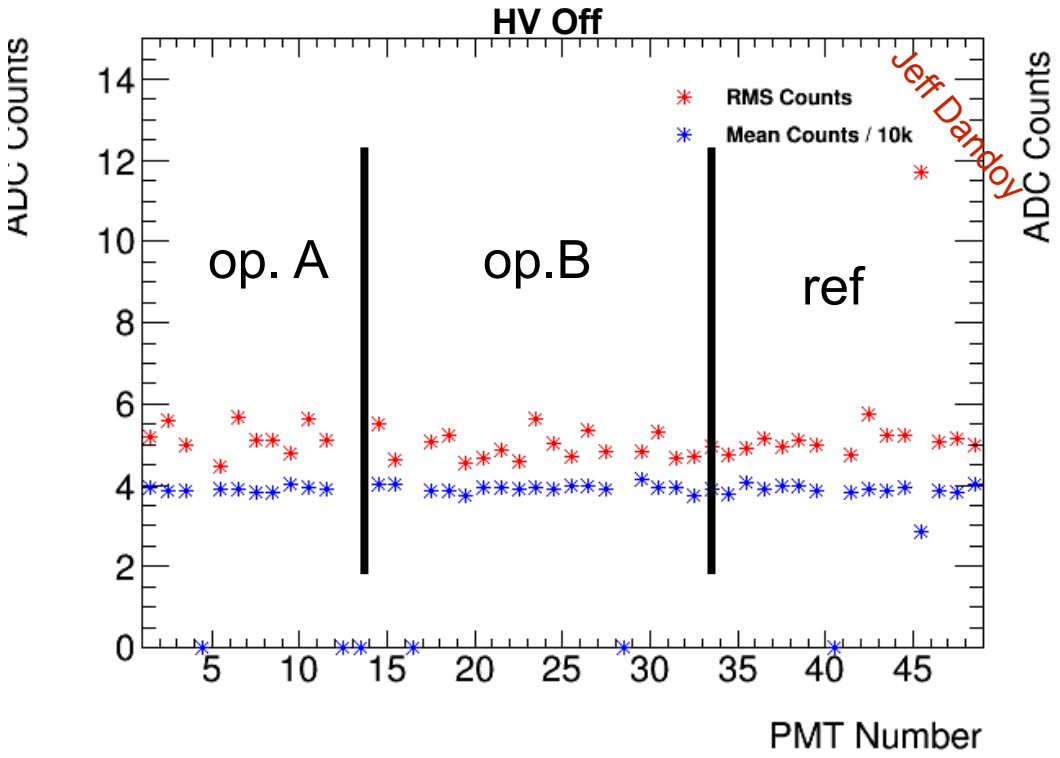
Block diagram for DCS integration for demonstrator

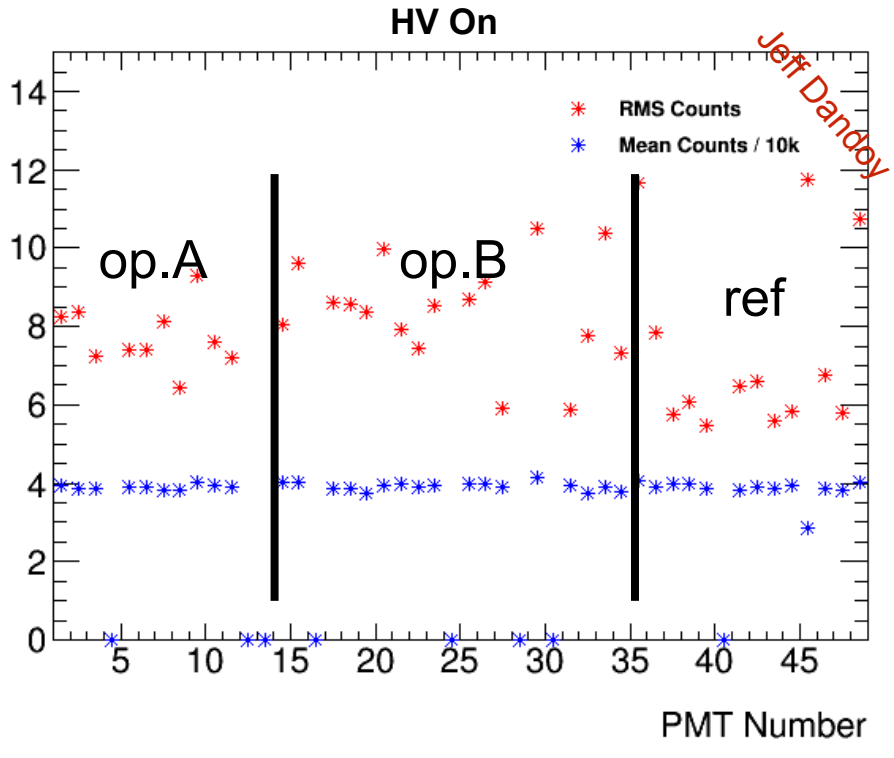




AM 900/x12-y3
i7-3555LE 16GB RAM

examples of performances: HV Options

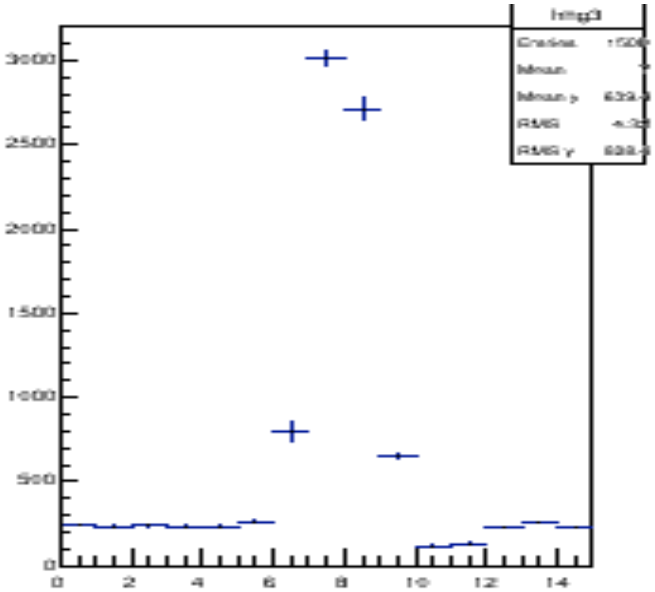




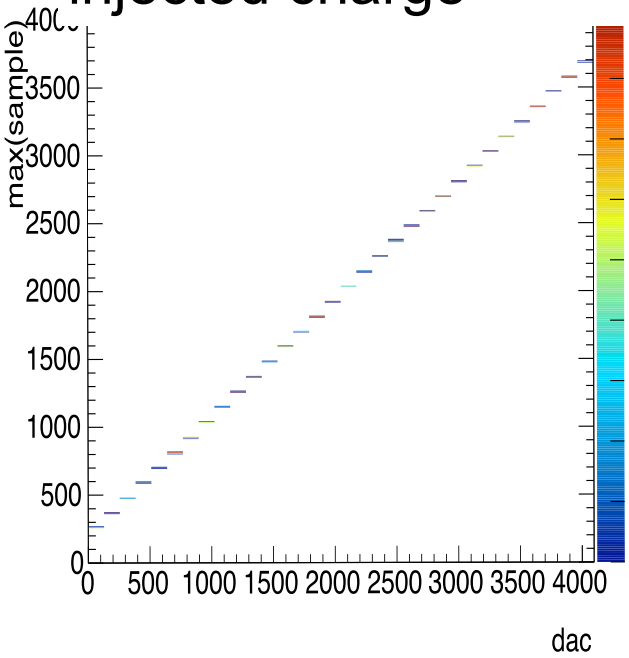
- preliminary comparisons shows very similar performances of the two HV regulation options in term of noise. Studies are ongoing.
- good stability

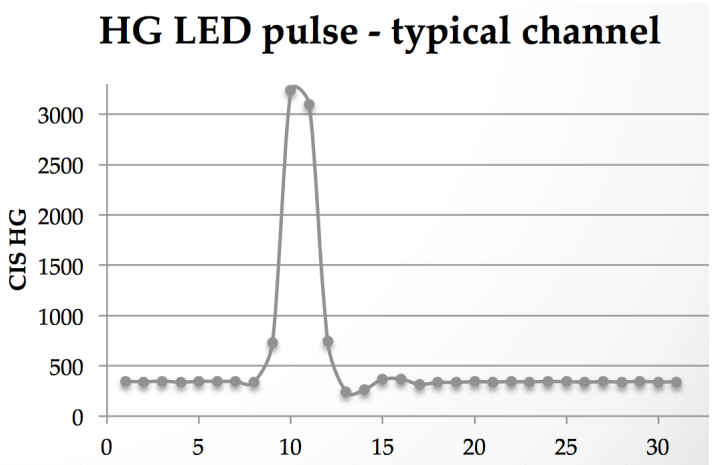
examples of performances

CIS signal pulse



CIS signal amplitude wrt injected charge



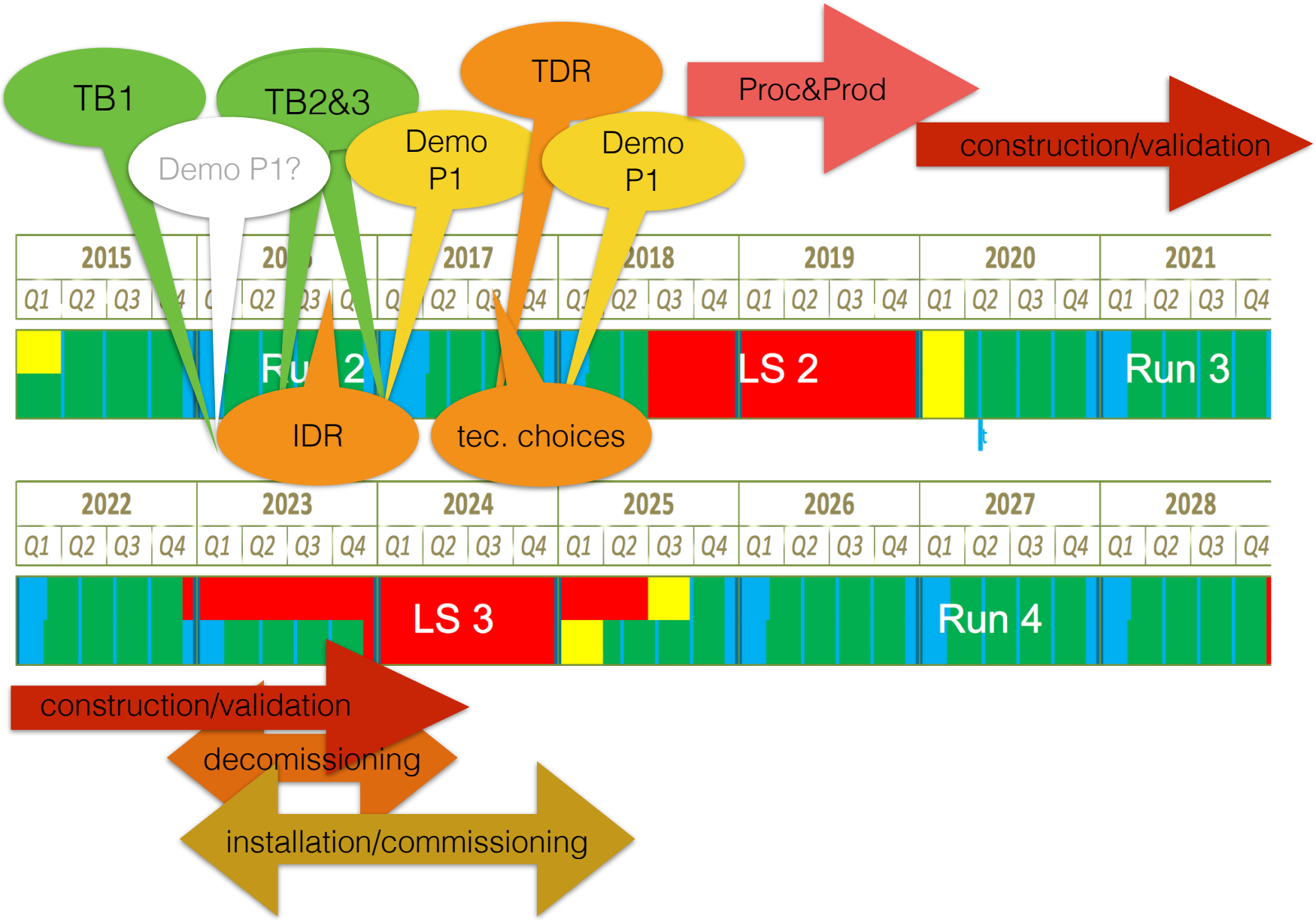



PULL&BEAR

Tile Upgrade R&D landscape

- FE boards: 3 options under study:
  - 3in1cards: (U.Chicago):
  - FATALIC (U. Clermont-Ferrand)
  - QIE (ASIC from FNL, optimised by ANL)
- Main Boards for services: MB(3in1), MB (common QIE,FATALIC)
- Optical Interface common to all options: Daughter Board (U. Stockholm)
- BE element: sROD (TPROM) (U. Valencia)
- HV Regulation boards: 2 Options under study:
  - HVOpto: (ANL)
  - HVRem: remote regulation in USA15 and distribution cables (U. Clermont-Ferrand)
- LVPS (ANL)
- Mini-drawer mechanics and tooling: (U.Barcellona,U.Clermont-Ferrand,ITIM Cluj)

milestones


TB1
TB2&3
Demo P1?
TDR
Demo P1
Demo P1
Proc&Prod
construction/validation
2015
2017
2018
2019
2020
2021
Q1 Q2 Q3 Q4
LS 2
Run 3
IDR
tec. choices
2022
2023
2024
2025
2026
2027
2028
LS 3
Run 4
construction/validation
decomissioning
installation/commissioning

Summary

- The Tile upgrade program for phase-II is well advanced.
- few alternative choices need to be fully evaluated testing prototypes in the lab, under beam tests
  - The first complete hybrid prototype (SD+sROD) originally target for insertion into ATLAS at the end of LS1 is under extensive testing in Bldg.175 LAB.
- will move to to the Test beam at the SPS in Oct 2015
  - additional mini-drawer prototypes with the different front end options are expected to join the testing during 2015 and 2016
- Aim for ATLAS review and successful insertion of the demonstrator into ATLAS in Dec. 2016

Backup

Radiation tests

Status of the Radiation Testing

Gary Drake

- Status of Testing → No changes since Valencia meeting…

	TID	NIEL	SEE	
COTS regulators	Done - OK	Not done	Not done	Need different -5V
3-in-1	Preliminary	Pending	Preliminary	More testing needed
Main board	Not done	Pending	Not Done	Size limitations
Daughter board	Not done	Pending	Done – OK	More testing needed
Modulator	Done – OK	Pending	Done – OK	Good to go
HV_Opto	Done – OK	Done – OK	Done – OK	Good to go
LVPS	Done (v7.5)	Done (v7.5)	Done (v7.5)	Needs full testing
Adders	Not needed	Not needed	Not needed	Testing not needed
Active bases	Done	Done	Not needed	Good to go
FATALIC	Not done	Not done	Not done	Not started
QIE	Not done	Not done	Not done	Not started

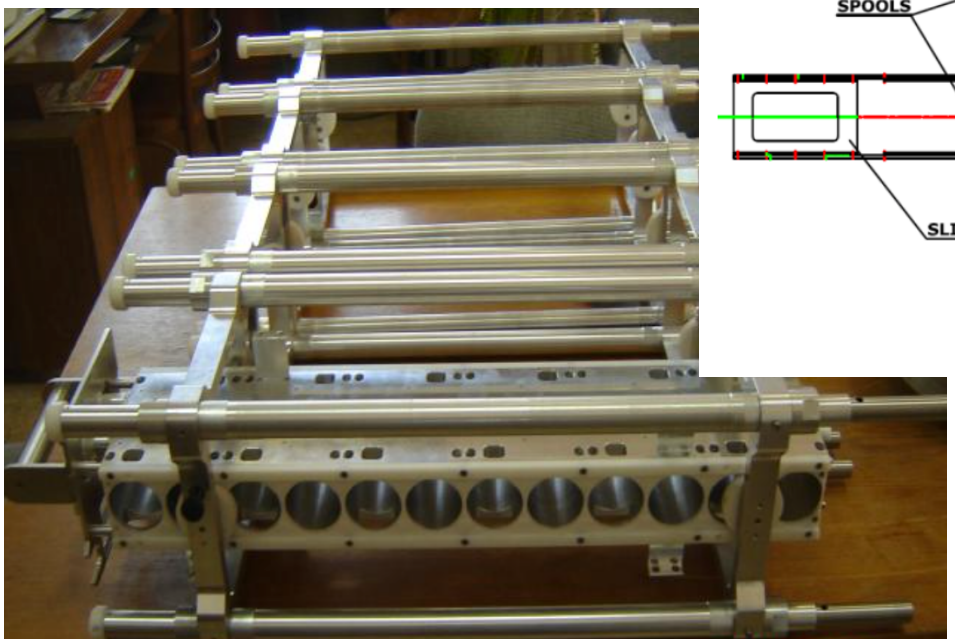
Status of the Radiation Testing – TileCal Upgrade Meeting – Feb. 11, 2015

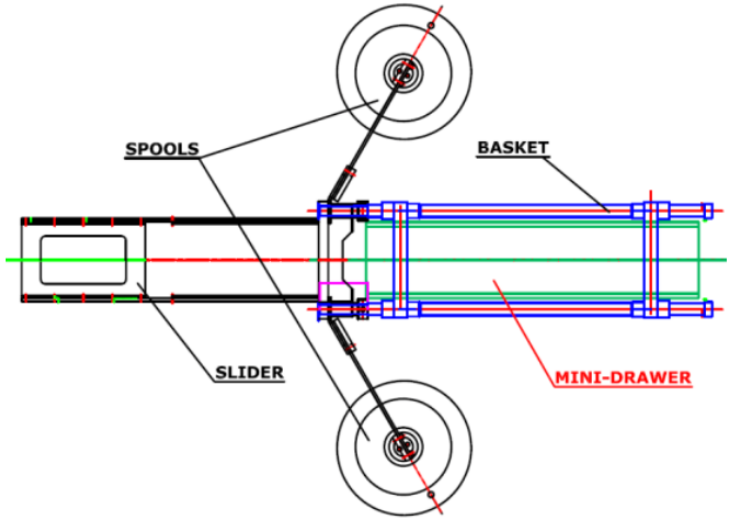
2

MD mechanics and tooling

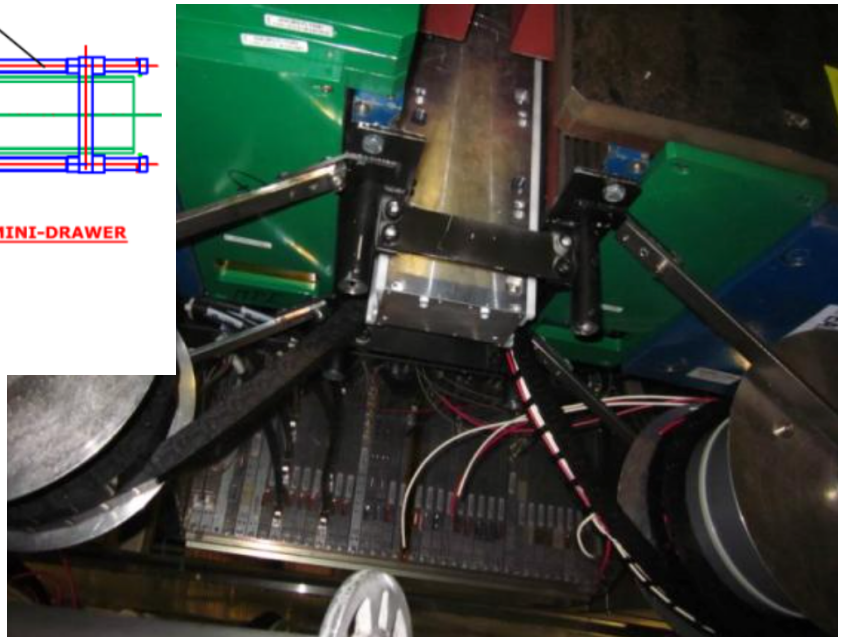
- One set v.1 and two v.2 were produced and tested. Documentation in EDMS.
  - one currently used in the demonstrator
  - New revision ongoing:integrating cooling plate for the DB and various improvements
- Tooling: Baskets, sliders, spools, v.3 produced and tested at CERN. v.4. being produced.
- Procedures for storage and manipulation being developed for installation of demonstrator in TB and ATLAS.

baskets and mini-drawer body





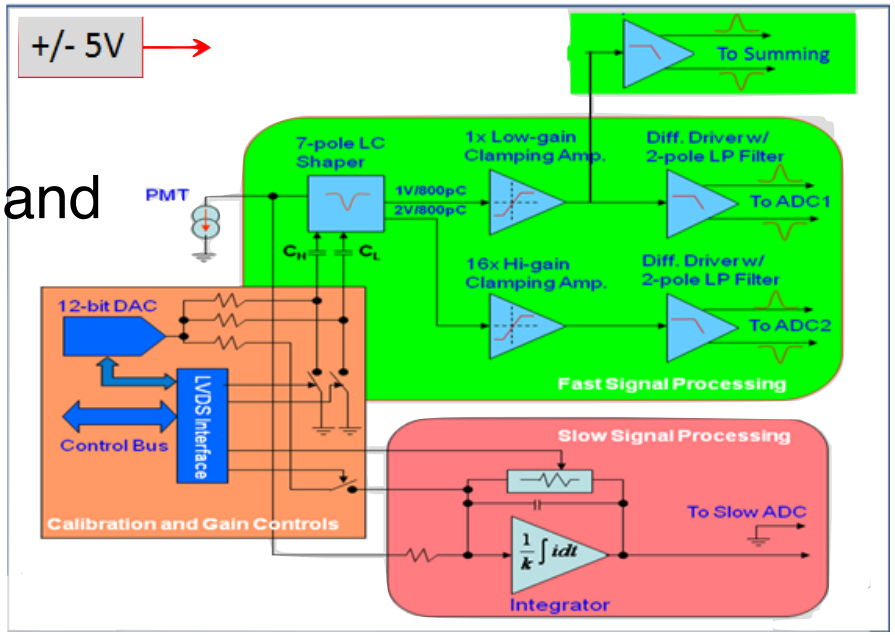
insertion test in ATLAS during LS1

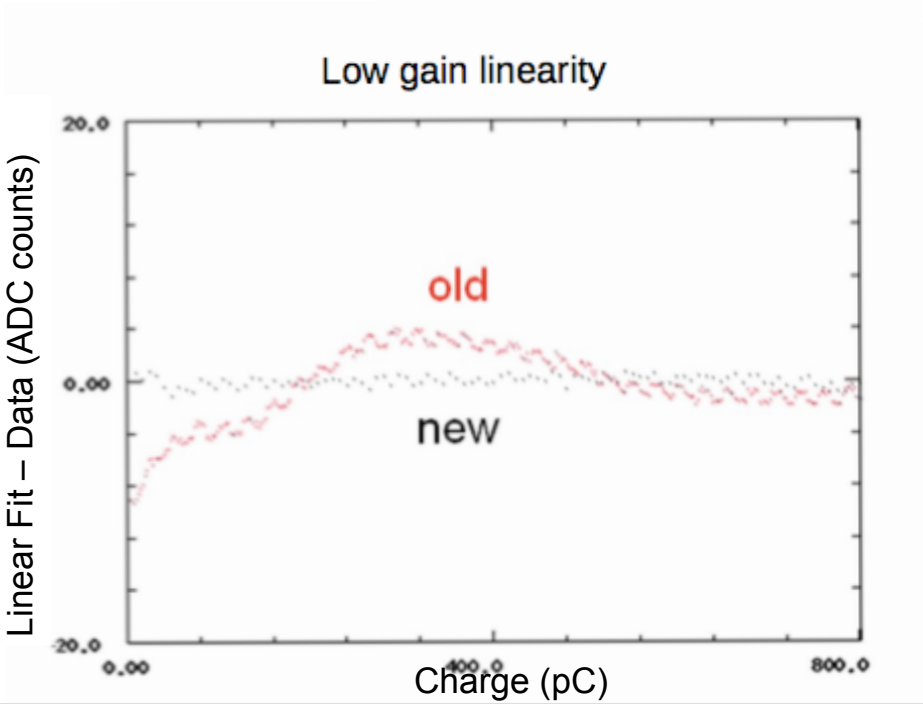


new 3-in-1 FE board

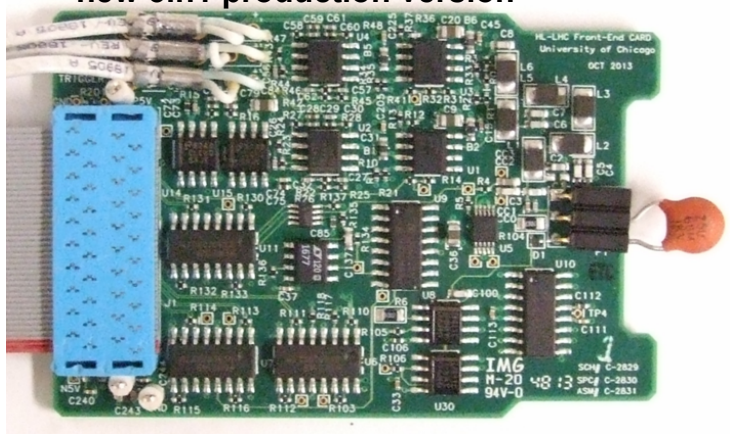
- based on current 3in1
  - improved noise
  - improved linearity
- design ready.
- first batch for demonstrator manufactured and qualified.
- minor revision for v.4 MB: cables length

Used in the hybrid demonstrator,since provide analog output to the LVL1 trigger



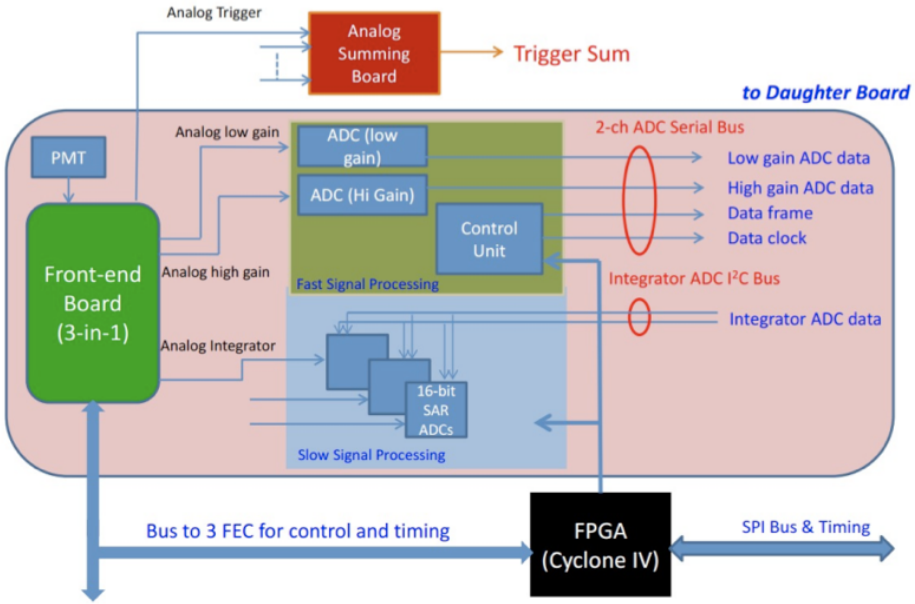


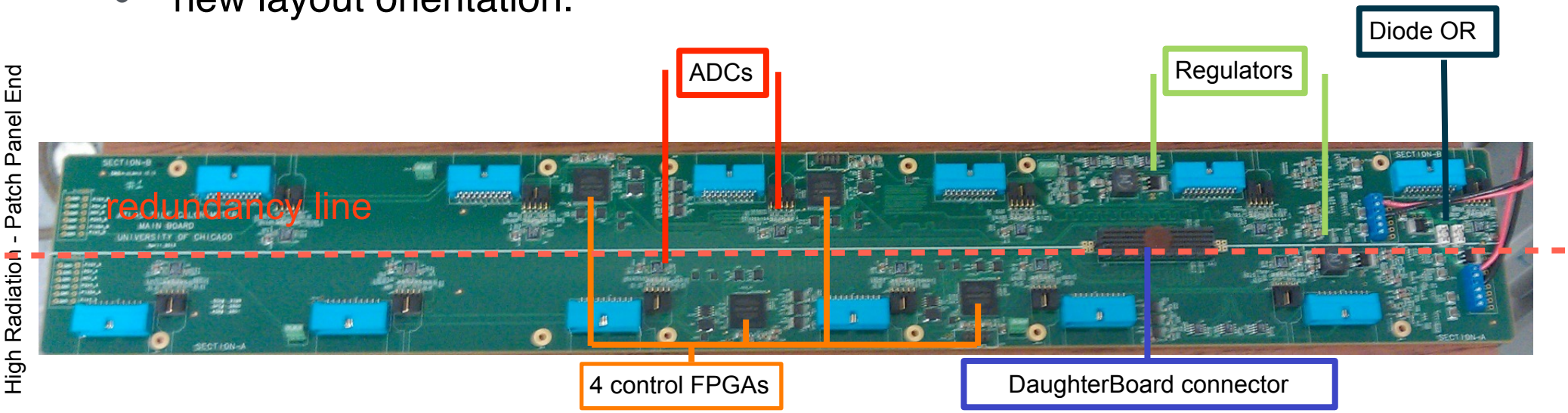
new 3in1 production version



Main-board for new 3-in-1 FEBs

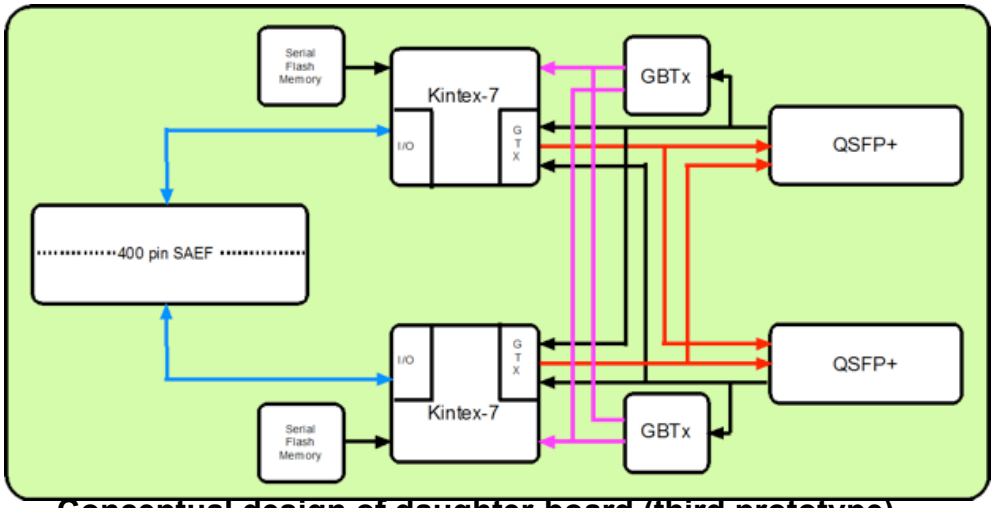
- clock distribution, control and monitoring of 12 FEBs (6 on each side)
- 8 pieces manufactured in v.3 and fully validated.
- Used in demonstrator prototype and all the test setup labs
- v.4 ready to produce 10:
  - improved synchronisation (serialization)
  - new definition DB-MB FMC connector.
  - new power connectors
  - new layout orientation.



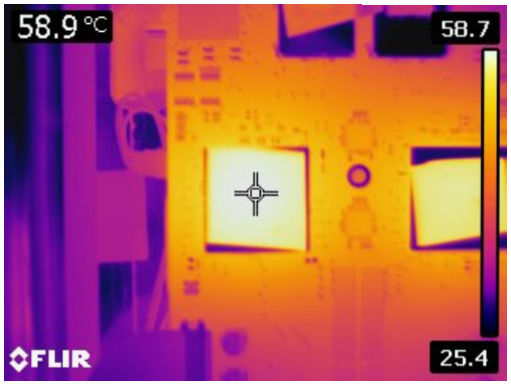


Daughter-board

- The Daughter-board provide high speed communication with the back-end electronics
- 8 units of the v.3 produced and used in demonstrator and in the other labs.
- not ready to use the GBTx chip to recover the clock.
- external jitter cleaner not fully debugged
- noise maybe causing instability. investigating.
- design revision v.4 ongoing.
- New board expected in August



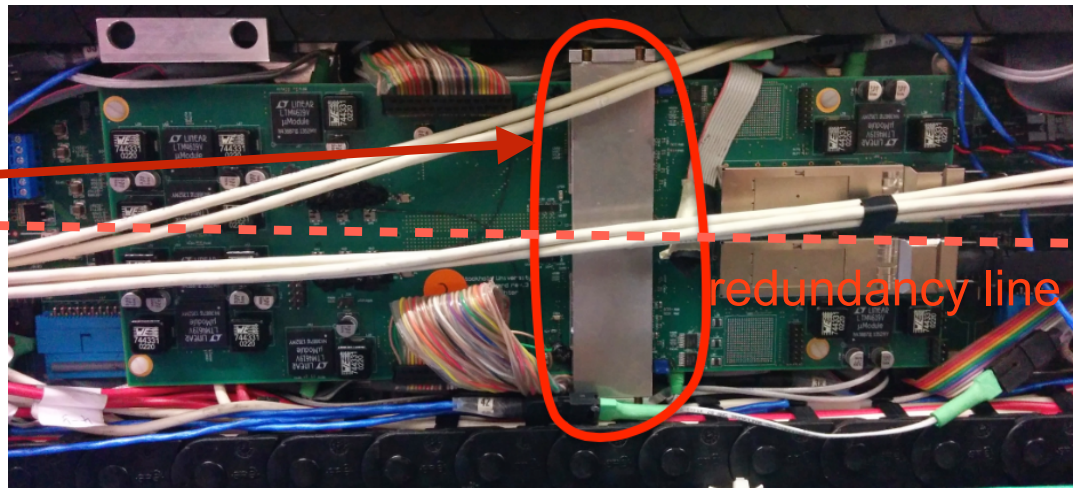
Conceptual design of daughter-board (third prototype)



Infra-red images showing two programmed FPGAs

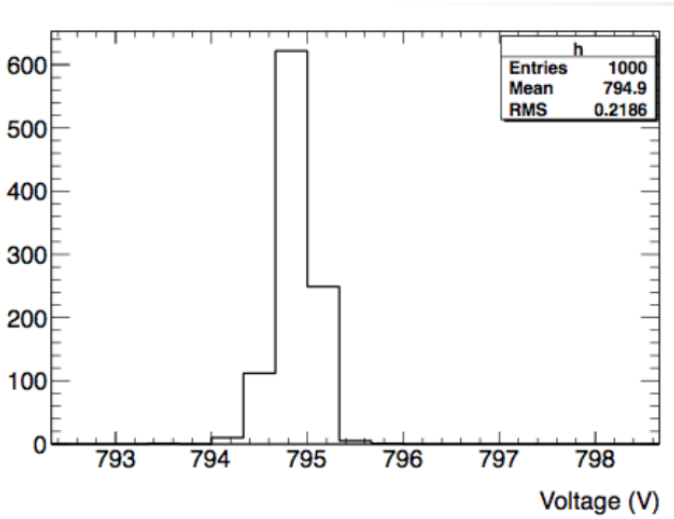
cooling bridge to the chassis
Temp now ~ 30

daughter-board v.3 with cooling bridge

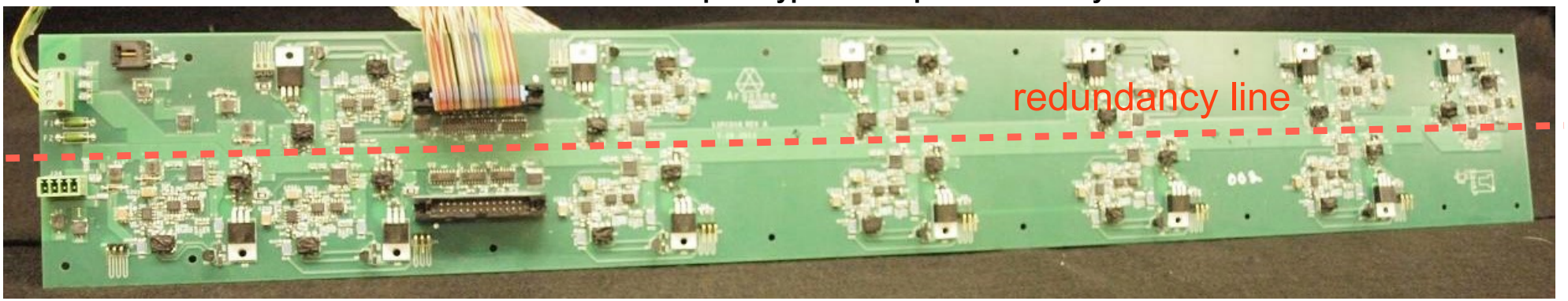


High voltage regulation and distribution

- two options under investigation:
  - HVRem: the existing local regulation system is moved to USA15 and individual cables are routed to the PMTs. First prototype built, under testing.
  - HVOpto: largely based on the existing system use Kintex-7 FPGA in the daughter board for control of HV settings and monitoring
  - Introduce possibility of switching on/off individual PMTs
- new HV (active) dividers ready.

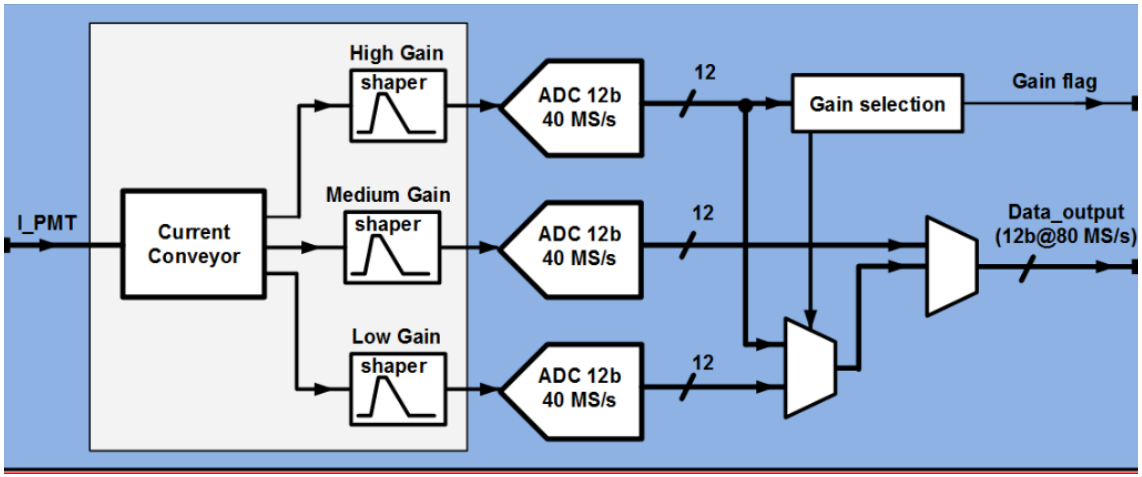


First prototype of HVOpto boa.

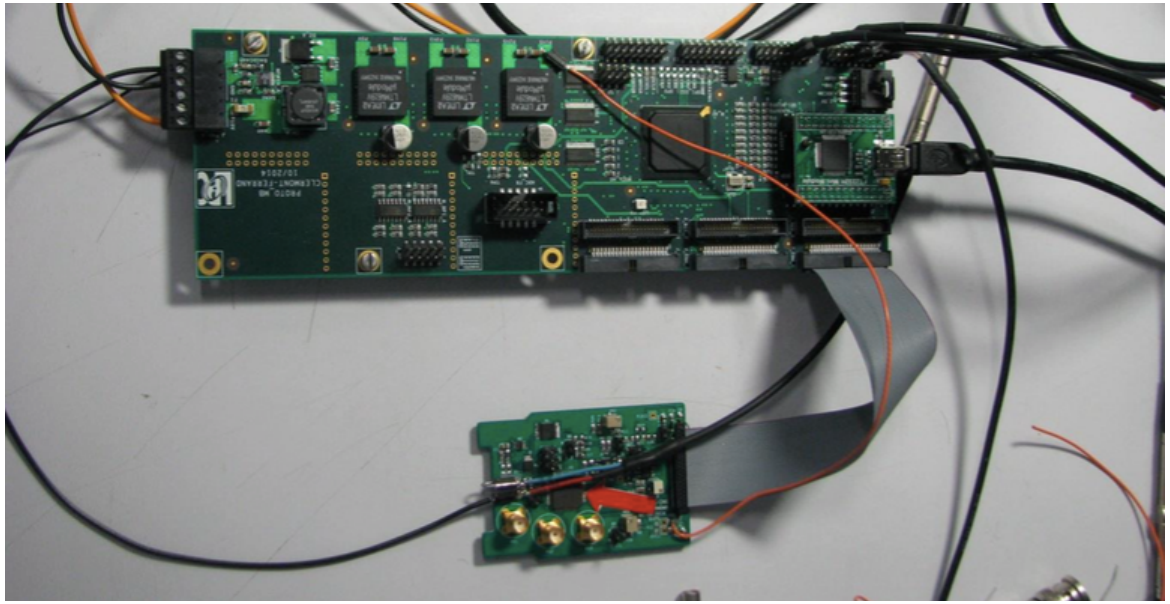


Allin1 FE boards (Fatalic)

- Combined ASIC solution
- Current conveyor and shaping stage with 3 different gain ratios (1, 8, 64)
- 12-bit pipelined ADCs at 40 MHz operation
- Status:
- FE boards FATALIC v.4 under testing using a special DAQ board
- MB for services currently under design.
- integration in the demonstrator readout possible in the summer



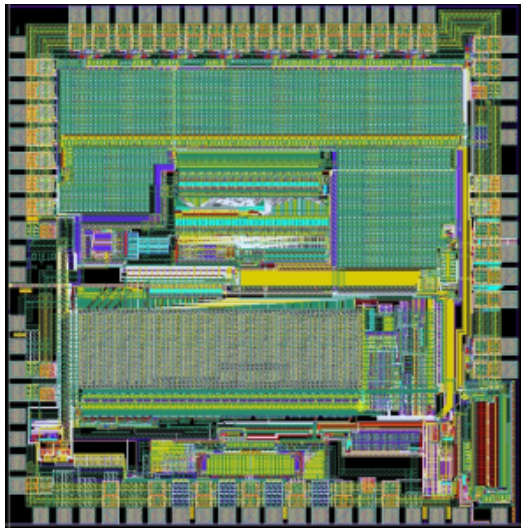
First prototype of ALLin1 FE board with FATALIC v.4



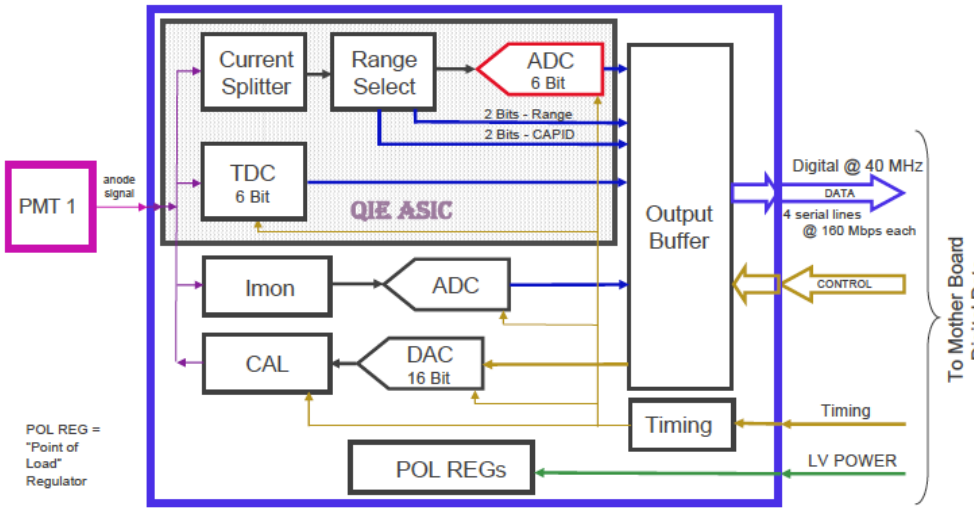
Allin1 FE boards (QIE)

- Charge Integrator and Encoder (QIE) chip from Fermilab
- Current splitter with multiple ranges and gated integrator + on-board flash ADC at 40 MHz operation
- 17 bit dynamic range in 10 bits
- Dead-timeless digitization (No pulse shaping)
- Status:
- 40 chips in hand
- integration in a FEB and DAQ development aiming at beginning of 2016

QIE v12



A Conceptual Design of the QIE Front End Board



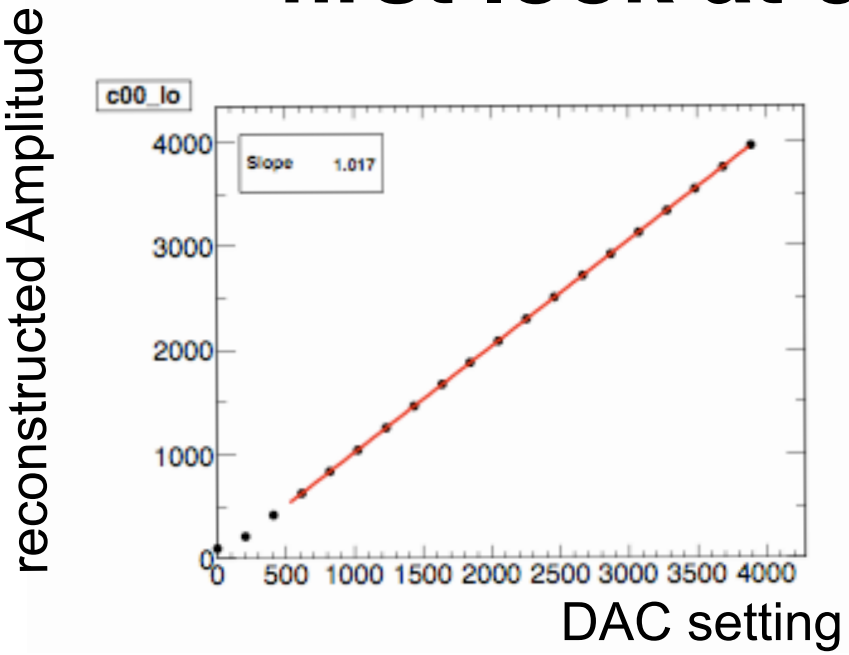
Plans

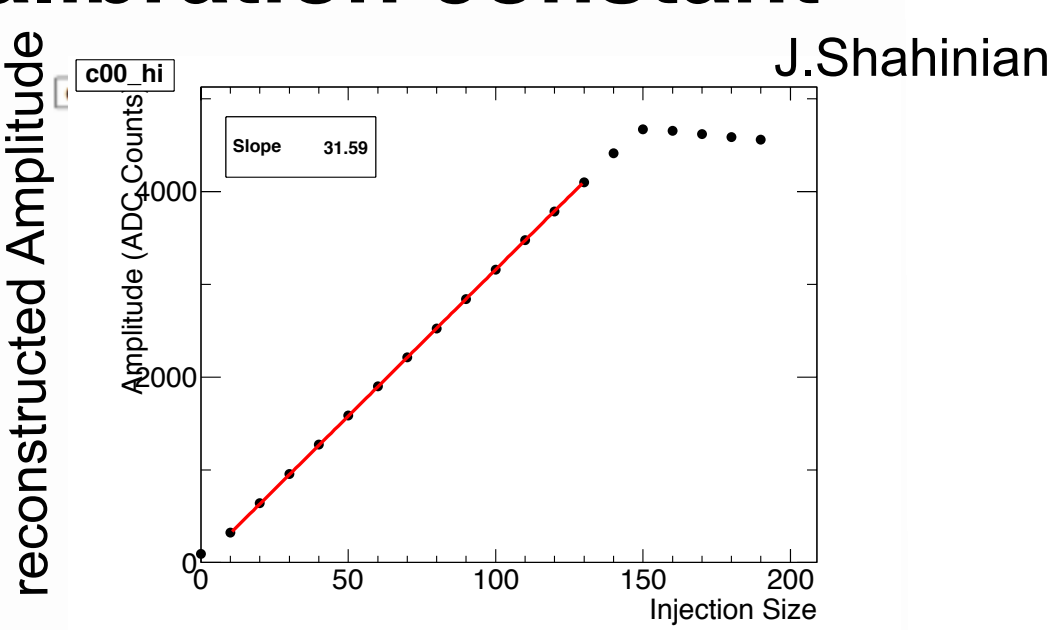
- Demonstrator prototype v.3 as installed in bldg 175:
  - continue the validation and the integration into the current ATLAS DAQ/DCS infrastructures:
  - use of TTC clock, achieve zero errors in transmission.
    - if no showstoppers are found by the end of summer, we plan to complete the ATLAS review and be ready to insert in the detector at the next possible occasion.

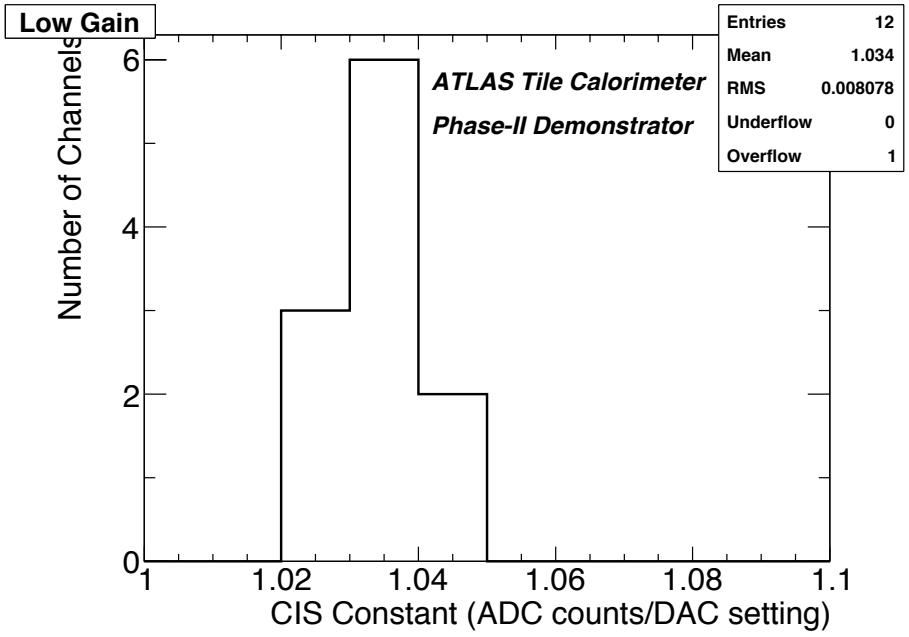
- Test beam campaign for the evaluation of the 3 FE options targeting v.4 components:
  - TB period in Oct 2015 confirmed. Organisation and setup of infrastructures already started.
  - Likely only one options will be fully debugged and ready for 2015.
  - two other periods in 2016 (beginning,end) to complete the studies.
- Integration test into TDAQ prototype (FELIX) as soon as available.
- IDR expected second half 2016
- TDR expected second half 2017

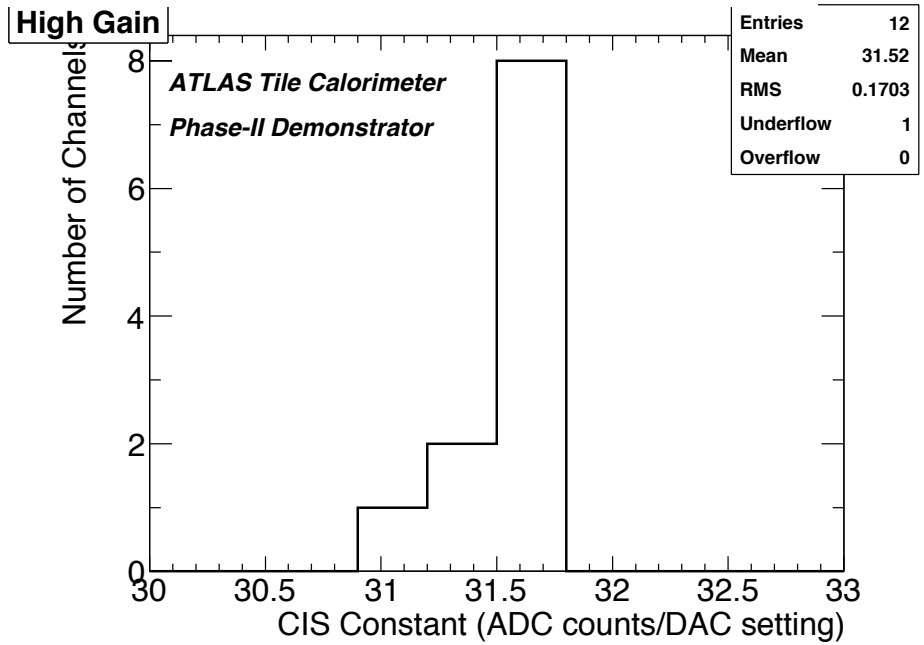
Basic operation tests
first look at calibration constant

J.Shahinian



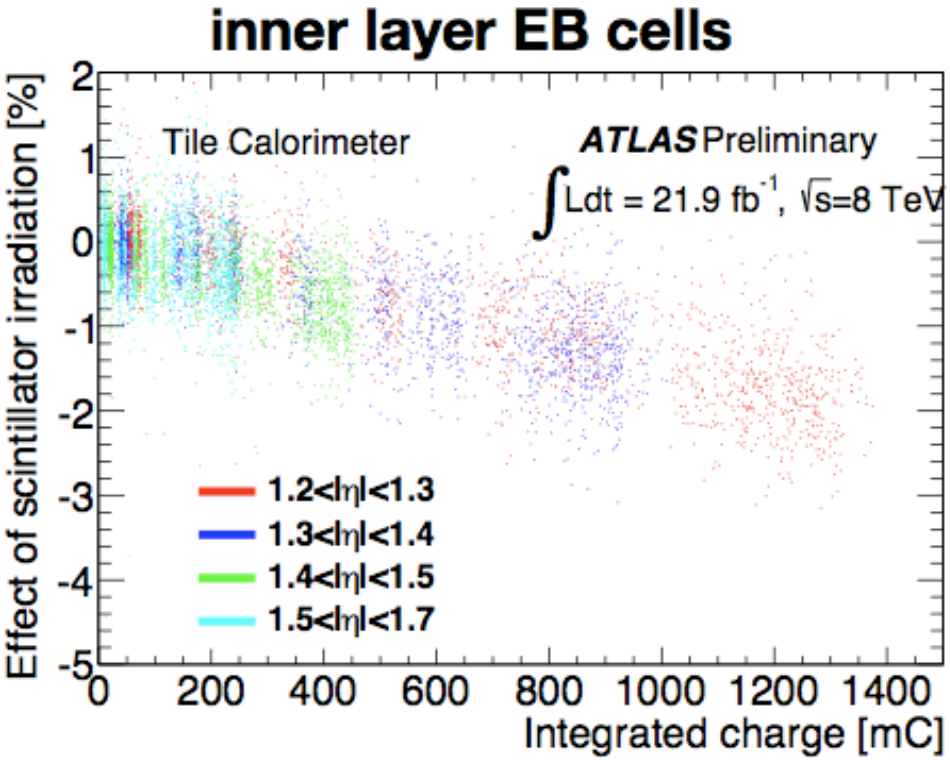


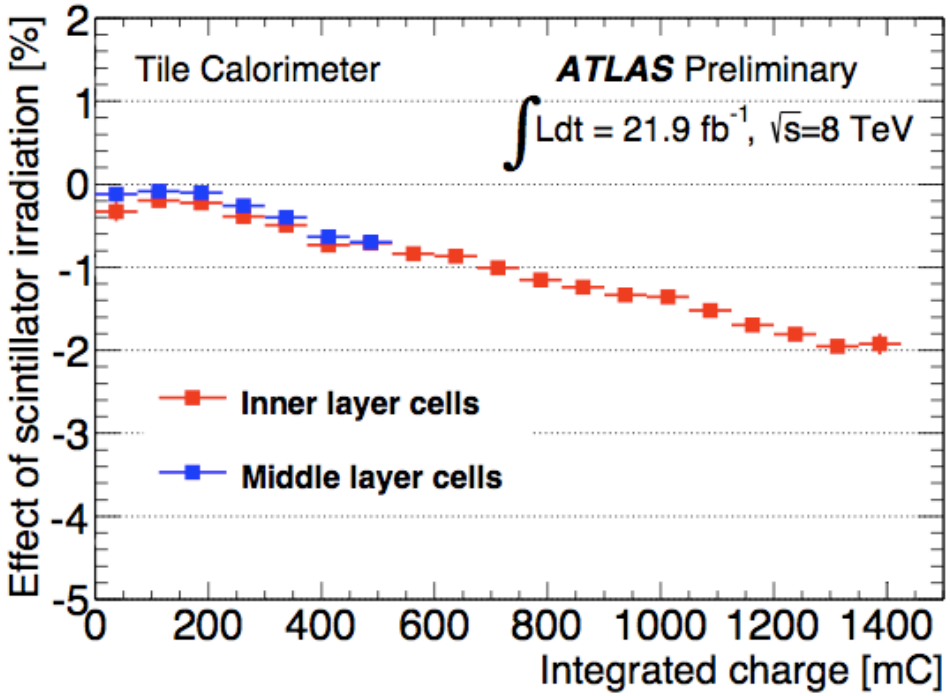




Irradiation effects on scintillator

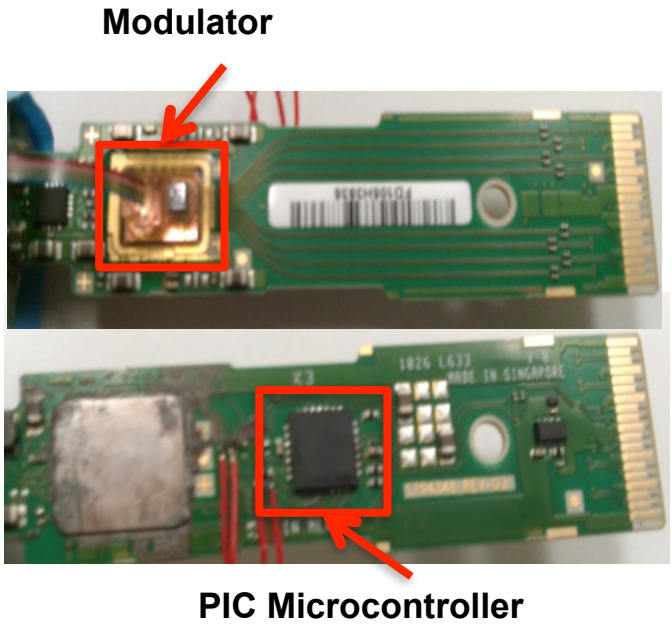
- difference between the Cs (Minimum Bias) and Laser response is interpreted as the effect of the irradiation on the scintillator. ≤ 2%for the worst case cells
- Cells light budget is fairly large (~80 phe/GeV), a factor X2 loss is expected not to be critical. Detailed study ongoing

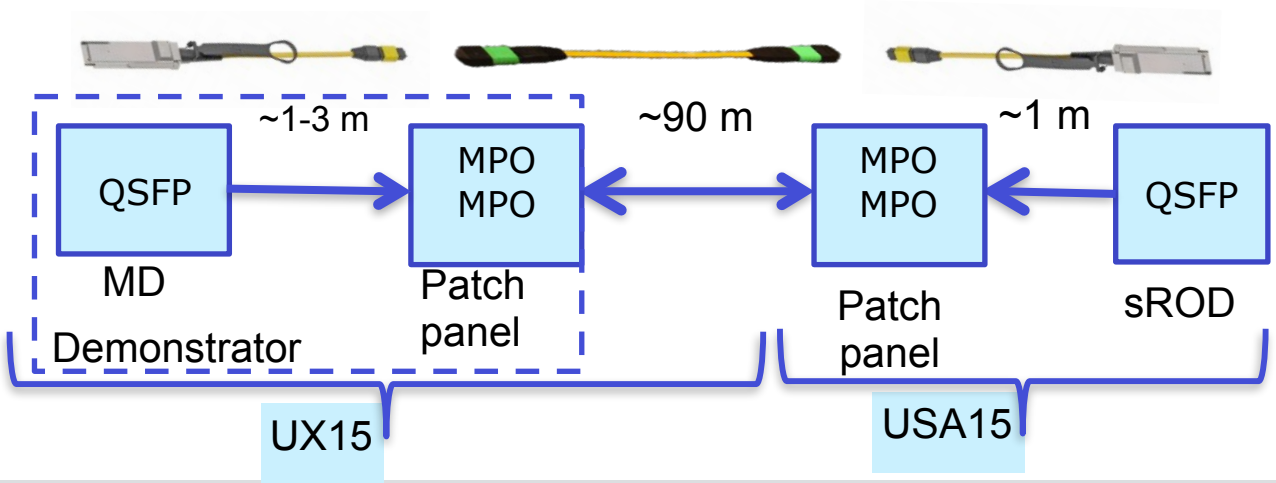




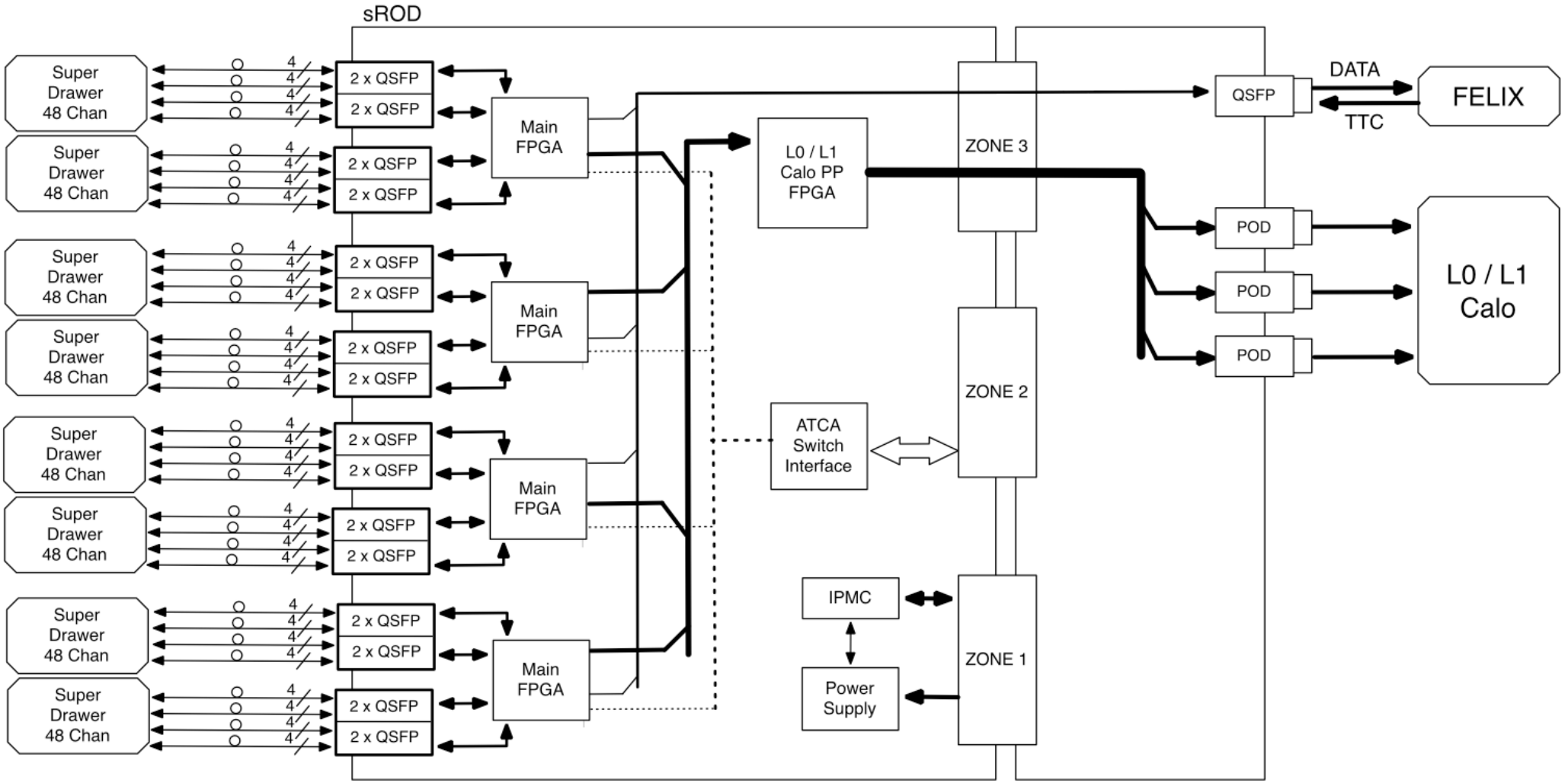
Read-out links

- 8 read-out links/super-drawer: 1+1 (redundancy) x 4 mini-drawers
- Luxtera Active Optical links:
  - 4 bi-directional channels: 1-14 Gbps/ch
  - excellent error rate: BER < 10^{-18} (~1err/3y)
- Made out of 130 nm Silicon On Insulator CMOS
- TID: tested up to 165 kRad passed but the PIC(used for configuration) fail at ~20 kRad. Replacement with an FPGA under investigation.
- SEU: tested under fluence of 1.2×10^{12} p/cm^2 operating at 10Gbps show ~0 Tx errors, few Rx errors. Still under investigation. Probably ok.

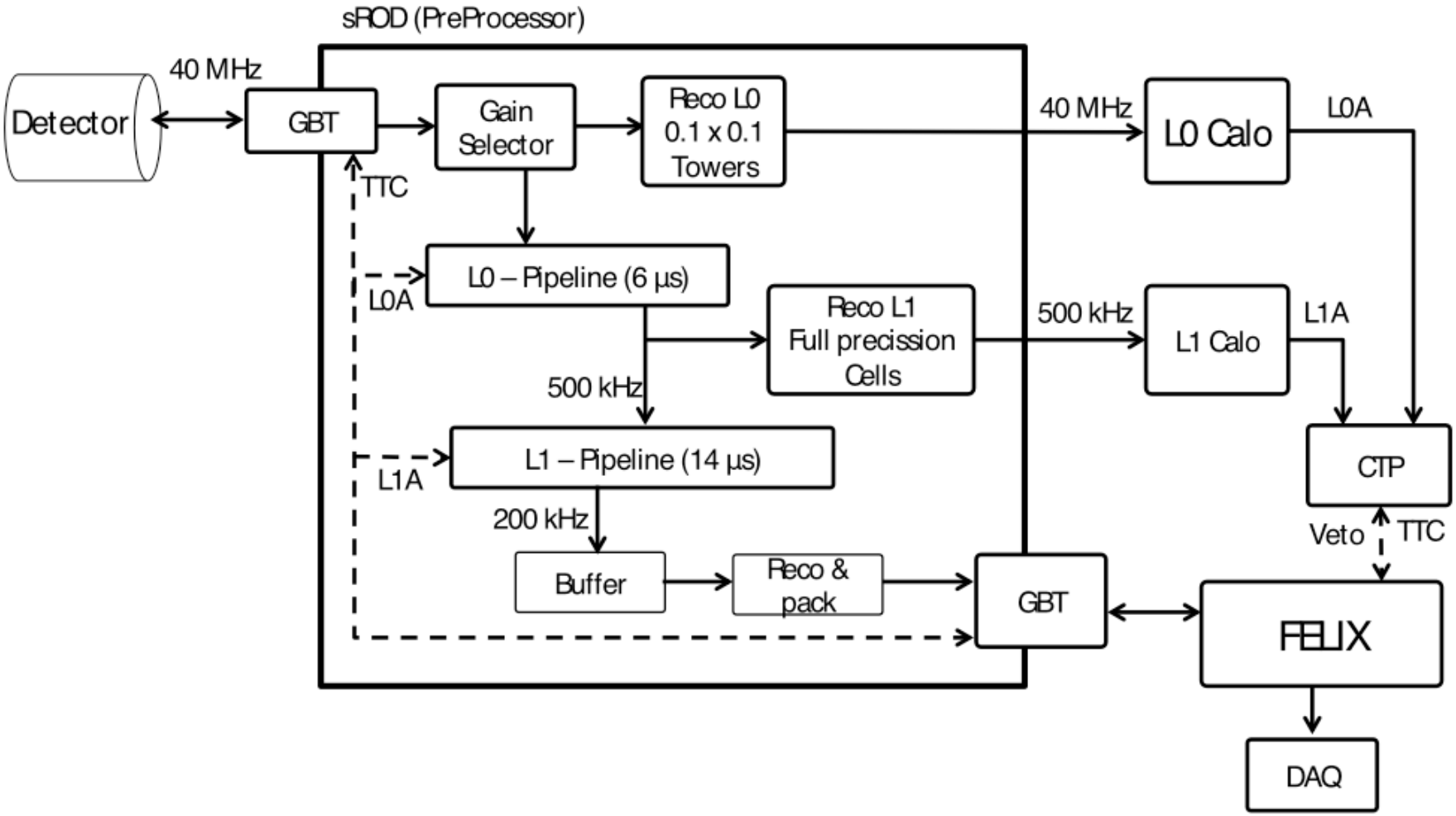




Possible layout for sROD



Readout dataflow in Phase-II



A portable test-bench for upgraded electronics

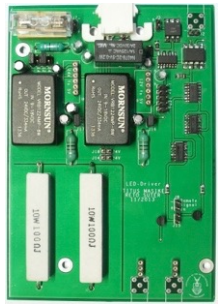
- A portable readout module for mini-drawers (Prometeo) is under development
  - Stand-alone test-bench to assess the QA of the electronics
- Hardware
  - Based on a Virtex 7 evaluation board
  - QSFP module provides optical connection
  - HV and LED driver boards test response of PMTs
  - 16 channel ADC mezzanine to digitize the output of trigger cables from previous test-bench
- Software
  - Based on IPbus, QT framework
  - Modular implementation to allow particular test implementation
- Status
  - All hardware components in hand,
  - Firmware under design

A Portable ReadOut ModulE for Tilecal ElectrOnics
PROMETEO

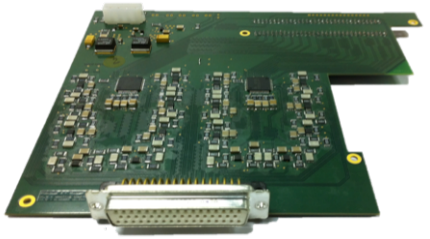
Virtex7 evaluation board

QSFP FMC module

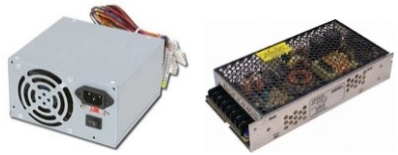
HV PS



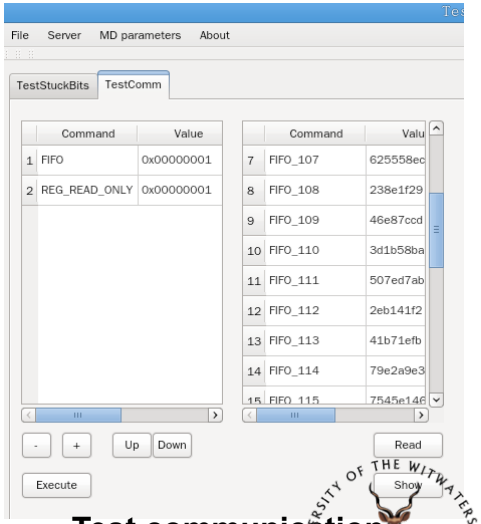
LED driver



16 channel ADC (hybrid demonstrator only)



System power supply (commercial ATX + 24V)

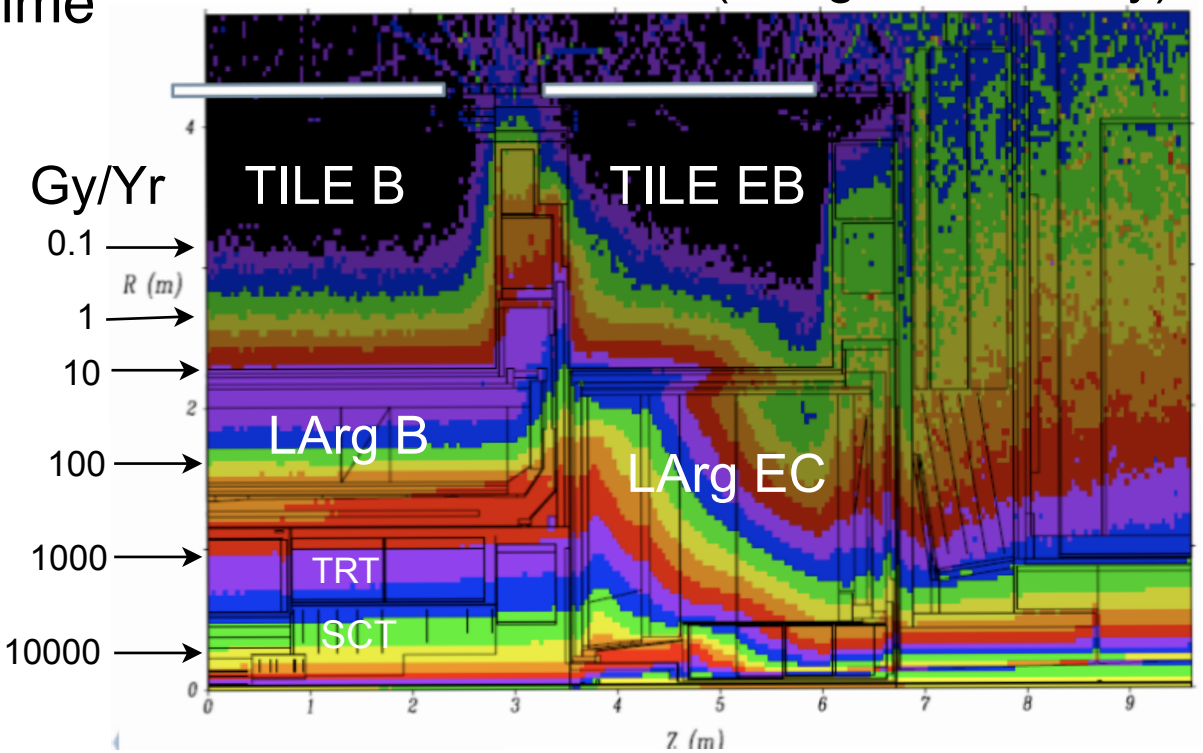


Test communication software panel

Motivations for the Tile upgrade

- LHC upgrade in 2023 aim to a luminosity X5-10 increase
  - better radiation tolerance is desirable
  - increased interaction rate demand for a better precision and finer granularity in the trigger
- ageing of component
  - exceeding the design lifetime
- improve the reliability
  - reduce/simplify the maintenance needs
- improve the accessibility
  - ALARA considerations

TID simulation (design Luminosity)



Phase 2 Radiation Tolerance Requirements (Estimate), TileCal HV_Opto					
Type	Simulated Dose/Yr	Simulation Safety Factor	Low Dose Rate Safety Factor	Lot Variation Safety Factor	Total 10 Year Operation
TID	8.13E-01 Gy/yr	1.5	5	4	2.44E+02 Gy
NIEL	7.62E+10 n/cm^2/yr	2	1	4	6.10E+12 n/cm^2
SEE	1.85E+10 p/cm^2/yr	2	1	4	1.47E+12 p/cm^2